ECE Department

3rd BOS File

D.N.R. COLLEGE OF ENGINEERING & TECHNOLOGY
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Ph: 08816-221238 Email: dnrcet@gmail.com website: https://dnrcet.org
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

CIRCULAR

This is to inform to all the BoS members of ECE department, the 3rd Board of Studies (BoS) meeting for the A.Y:2026-27 will be held on 09/01/2026, Friday at 10:00 AM in the MPMC Lab in on-line mode. All the BoS members are invited to attend the meeting and the link for on-line meeting will be shared through mail ID.

Agenda

1. **Welcome Speech by the Chairperson.**
2. **Introducing the members of the Board of Studies.**
3. **To discuss and finalize the proposed III B. Tech. I & II Semester Course structure and Syllabus of DR24 Regulations.**
4. **To discuss and finalize the proposed M. Tech. Course structure and Syllabus of DR25 Regulations.**
5. **Ratification of Course Objectives and Course Outcomes for the proposed Curriculum.**
6. **Finalization of Model Question Papers and List of Paper Setters.**
7. **Any other item with the permission of the chair**

Head of the Department & BoS Chairman

Copy To:

1. **The Members of the BoS**
2. **The Principal**
3. **The Dean (Academics)**
4. **To the Office File**

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Description	Designation in Committee	Name(s) of the Member(s)/Nominee(s)
Head of the Department concerned	**Chairperson**	Dr. K. Venu Gopal
One expert is to be nominated by the Vice-Chancellor from a panel of six recommended by the Autonomous College Principal	**Member (University Nominee)**	Dr. B. T Krishna, Professor, ECE Department, University College of Engineering, Kakinada, AP-533003. e-mail: tkbattula@jntucek.ac.in Mobile: 9502770755.
Two subject experts from outside the parent University are to be nominated by the Academic Council.	**Member (Subject experts from outside the parent University)**	Dr. N. Udaya Kumar, Professor & HOD, ECE Dept, SRKR Engineering. College (Autonomous), Bhimavaram-534202, e-mail: nuk@srkrec.ac.in Mobile: 9440354093.
	Member (Subject experts from outside the parent University)	Dr. P. Srinivasa Rao, Assoc. Professor, ECE Dept., St. Anna's College of Engineering & Technology (Autonomous), Chirala-523187 e-mail: psraoece@gmail.com Mobile: 6281266754.
One representative from the industry/corporate sector/allied areas to be nominated by the principal	**Member (Industrial Expert)**	Mr. Sriramulu Govada, Design. Technical Officer 'A', DRDO, Visakhapatnam, e-mail: sriramgovada@gmail.com Mobile: 9492126360.
One member of the College alumni to be nominated by the principal	**Member (College alumni)**	Mrs. I. Pavani, 2016-20 Batch, Roll No.169P1A0416, e-mail: pavaniindukuri123@gmail.com, Mobile No: 63039 84842.

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Experts from outside the Autonomous College, whenever special courses of studies are to be formulated, are to be nominated by the principal	**Member** **(Experts from outside the Autonomous College)**	NA
All faculty members of the Department	**Members**	Dr. Nekkanti Venkata Rao Dr A.Purna Ramesh Dr.S. Ravi chandra Mr. Kopalli Venkanna Naidu Mr. Kurma Sekhar Babu Mr. S Satish Kumar Mrs. N Mary Leena Mr.M. Venu Mrs.K Indira Priyadarsini Mrs. B. Nagamani Mrs. Rosey Sharon Mr. P. Gopala Swami Mr. Rakesh Patnaik Mrs. P. Srivalli Mr. Vendra Bhavani Durga Mrs. K. Durga Mr.B. Sudhakar Mrs. K. Vanaja Mrs. U. Sai Mounica

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

Dr. B. T Krishna,
Professor, ECE Department,
University College of Engineering,
Kakinada, AP-533003.

Dear sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

We take the privilege in inviting you for the Board of Studies (BoS) 3rd meeting of the ECE department, DNR College of Engineering & Technology(9P) as a Subject Expert from outside the parent university. It is proposed to discuss and finalize the following for the A.Y. 2026- 27.

1. **Welcome Speech by the Chairperson.**
2. **Introducing the members of the Board of Studies.**
3. **To discuss and finalize the proposed III B. Tech. I & II Semester Course structure and Syllabus of DR24 Regulations.**
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7. **Any other item with the permission of the chair**

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Kindly accept our invitation and make it convenient to attend the Board of Studies meeting.

Yours Sincerely,

K Venu Gopal

(Dr. K. Venu Gopal)

HoD and Chairman BoS.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

To

Dr. N. Udaya Kumar,
Professor, ECE Department,
SRKR Engg. College (Autonomous),
Bhimavaram, AP-534202.

Dear Sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

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Bhimavaram,
Dt: 07/01/2026.

To

Dr. P. Srinivasa Rao,
Assoc. Professor, ECE Department,
St. Anna's College of Engineering & Technology (Autonomous),
Chirala, AP – 523187.

Dear sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

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K Venu Gopal

(Dr. K. Venu Gopal),

HoD and Chairman BoS.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

Mrs. I. Pavani,
2016-20 Batch,
Roll No.169P1A0416,
Bhimavaram,
AP-534202.

Dear sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

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k Venu Gopal

(Dr. K. Venu Gopal)

HoD and Chairman BoS.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

Mr. Sriramulu Govada,
Design. Technical Officer 'A',
DRDO, Visakhapatnam,
AP-530027.

Dear sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

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Kindly accept our invitation and make it convenient to attend the Board of Studies meeting.

Yours Sincerely,

K Venu Gopal

(Dr. K. Venu Gopal)

HoD and Chairman BoS.

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

1 message

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 12:59 PM
To: tkbattula@jntucek.ac.in

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

--
With Warm regards
HOD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Dr.B.T Krishna.pdf
364K

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

2 messages

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 12:58 PM
To: Uday N <udayvas2005@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

--
With Warm regards
HOD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Dr.N.Uday Kumar.pdf
345K

Uday N <udayvas2005@gmail.com> Thu, Jan 8, 2026 at 4:23 PM
To: ELECTRONICS <dnrcetece@gmail.com>

Ok sir.
All the best sir

with best wishes and regards
Dr. N. Udaya Kumar **M. Tech, Ph. D, MISTE, MSIOI,MBMESI,MSEMCE(I),FIE,FIETE**
Senior Member IEEE(SMIEEE),
Professor and Head, Department of ECE,
SRKR Engineering College,
Bhimavaram
Ex-Secretary, IEEE Comsoc/SP Societies Joint Chapter, IEEE Vizag Bay Section
Ex-AP State Committee Member (IE)- ET Division
Mobile: 9440354093(Whatsapp)
:6300465439(Whatsapp)
[Quoted text hidden]

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 1:01 PM
To: Pavani Indukuri <pavaniindukuri123@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

--
With Warm regards
HOD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

I.Pavani.pdf
398K

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

1 message

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 12:55 PM
To: Srinivas Rao <psraoece@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

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With Warm regards
HoD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Dr.P.Srinivasa Rao.pdf
374K

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

1 message

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 1:01 PM
To: Sriram Govada <sriramgovada@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

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With Warm regards
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Mr.Sriamulu Govada.pdf
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Bhimavaram,
09/01/2026.

Ref: DNRCET/ECED/2025-26/BOS-MOM/1

Minutes of Meeting (MOM) of the Board of Studies (BOS)

The 3rd Board of Studies (BoS) meeting for the Electronics & Communication Engineering (ECE) Department took place on Friday, January 9, 2026, via Zoom in the MPMC Lab. The session focused on reviewing the proposed agenda and adopting key resolutions.

Meeting link

https://us06web.zoom.us/j/88650471236?pwd=sozL2jB9kdnblbXv6n0XF4t6oGuzel.

Agenda:

1. **Welcome Speech by the Chairperson.**
2. **Introducing the members of the Board of Studies.**
3. **To discuss and finalize the proposed III B. Tech. I & II Semester Course structure and Syllabus of DR24 Regulations.**
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5. **Ratification of Course Objectives and Course Outcomes for the proposed Curriculum.**
6. **Finalization of Model Question Papers and List of Paper Setters.**
7. **Any other item with the permission of the chair**

The following members attended the meeting:

Name(s) of the Member(s)/Nominee(s)	Designation in Committee	Signature
Dr. K. Venu Gopal	**Chairperson**	K. Venu Gopal
Dr. B. T Krishna, Professor, ECE Department, University College of Engineering, Kakinada, AP-533003. e-mail: tkbattula@jntucek.ac.in Mobile: 9502770755.	**Member** **(University Nominee)**	ON-LINE

Dr. N. Udaya Kumar, Professor, ECE Dept, SRKR Engineering. College (Autonomous), Bhimavaram-534202, e-mail: nuk@srkrec.ac.in Mobile: 9440354093.	**Member** **(Subject experts from outside the parent University)**	ON-LINE
Dr. P. Srinivasa Rao, Assoc. Professor, ECE Dept., St. Anna's College of Engineering & Technology (Autonomous), Chirala-523187 e-mail: psraoece@gmail.com Mobile: 6281266754.	**Member** **(Subject experts from outside the parent University)**	ON- LINE
Mr. Sriramulu Govada, Design. Technical Officer 'A', DRDO, Visakhapatnam, e-mail: sriramgovada@gmail.com Mobile: 9492126360.	**Member** **(Industrial Expert)**	ON-LINE
Mrs. I. Pavani, 2016-20 Batch, Roll No.169P1A0416, e-mail: pavaniindukuri123@gmail.com, Mobile No: 63039 84842.	**Member** **(College alumni)**	ON- LINE
Dr. Nekkanti Venkata Rao	**Members** **of the Department**	
Dr A. Purna Ramesh		
Dr. S. Ravi chandh		
Mr. Kopalli Venkanna Naidu		
Mr. Kurma Sekhar Babu		
Mrs.N.S.V.L. Sowjanya		

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Mr. K. Satish Kumar	**Members of the Department**	
Mrs. N Mary Leena		
Mr.M. Venu		
Mr. S. Apparao		
Mrs.K Indira Priyadarsini		
Mrs. B. Nagamani		
Mr. P. Gopala Swami		
Mrs. K. Krishna Deepika		
Mrs. P. Srivalli		
Mr. Vendra Bhavani Durga		
Mrs. K. Durga		
Mrs. U. Sai Mounica		
Mr.S. Joseph		
Mrs.P. Pardhavi		
Mr. P Narasimha Murthy		
Mr.V. Phani Kiran		
Ms.N. Sowjanya		
Ms.K. Uma devi		
Mr.G. Manikanta		
Mr.T Srinivas		
Mr.J.S.S. Ramaraju		
Ms. S.R..S. Anusha		
Ms.G. Chinnari		

The Principal of DNRCET opened the meeting by thanking the university nominee and all BoS members. Dr. K. Venu Gopal, Chairman of the ECE BoS, then took charge of the proceedings. The meeting concluded with the following key resolutions:

Resolutions:

Agenda Point 1: Welcome speech by the chairperson

Resolution: Dr. K. Venu Gopal, Chairman of the BoS, warmly welcomed all BoS members.

Agenda Point 2: Introduction of members

Resolution: The Chairman of BoS, Dr. K. Venu Gopal, welcomed all the members and introduced internal BoS members to external BoS members.

The meeting began with the III B. Tech curriculum presentation for semesters I & II.

Agenda Point 3: To discuss and finalize the proposed III B. Tech-I & II Semester ECE (Theory and Lab) courses of DR24 Regulations.

Resolution: After clearly discussing every unit of theory courses curses

III B. Tech-I Semester DR24 Syllabus (Theory & Labs)- including professional Electives curses 1. Analog & Digital IC Applications, 2. Digital communications, 3. Antennas and Wave Propagation,4. Digital System Design through HDL, 5. Optical Communications, 6. Electronic Measurements and Instrumentation, 7. Computer Organization and Architecture, 8. Analog & Digital IC Applications Lab, 9. Analog and digital communications Lab. 10. Applications of Lab view for Instrumentation & Communications, 11. Design of PCB & Antennas Lab.

III B. Tech-II Semester DR24 Syllabus (Theory & Labs)- including professional Electives curses 1. VLSI Design, 2. Microprocessors & Microcontrollers, 3. Digital Signal Processing, 4. Analog IC Design, 5. Satellite Communication, 6. Smart and Wireless Instrumentation, 7. Machine Learning, 8. Bio Medical Instrumentation, 9. Microwave Engineering, 10. Embedded Systems, 11. Artificial Intelligence, 12. VLSI Design Lab, 13. Microprocessors & Microcontrollers Lab, 14. Machine Learning Lab

List of Open Elective courses offered by department of ECE:

Pool 1: Open Elective 1 (Either of the 4 subjects)-

1. Electronic Devices and Circuits, 2. Signals and Systems, 3. Probability Theory and Random Variables, 4. Network Analysis

Pool 2: Open Elective 2 (Either of the 4 subjects)-

1. Linear and Digital IC Applications, 2. Principles of Communications, 3. Principles of Signal Processing, 4. Microprocessors & Microcontrollers.

Pool 3: Open Elective 3 (Either of the 4 subjects)-

1. Fundamentals of VLSI Design, 2. Digital Electronics, 3. Electronic Measurements and Instrumentations, 4. Optical Communications.

Pool 4: Open Elective 4 (Either of the 4 subjects)-

1. Principles of Cellular & Mobile Communications, 2. Fundamentals of Satellite Communications, 3. Embedded Systems, 4. Transducers and Signal Conditioning.

Annexure-A **(Enclosed Annexure-A).**

Agenda Point 4: To discuss and finalize the proposed M. Tech. Course structure and Syllabus of DR25 Regulations.

Resolution: After clearly discussing every unit of theory courses,

M. Tech DR25 I Semester Syllabus (Theory & labs)-1. including professional Electives curses 1.Mathematical Foundation for Communication Engineering, 2. Digital System Design, 3. Wireless Communications & Networks, 4. Software Defined Radio, 5. Optical Communication & Networks, 6. Radio and Navigational Aids, 7. FPGA and ASIC Design, 8. System Design with RTOS & Embedded LINUX, 9. System Design Using Verilog, 10. Digital System Design Laboratory, 11. Wireless Communications Laboratory, 12. Seminar.

M. Tech DR25 II Semester Syllabus (Theory & labs)-1. including professional Electives curses 1.Information Theory and Coding, 2. IoT & its Communication Protocols, 3. Embedded System Design, 4. Design for Testability, 5. MEMS, 6. System on Chip Design, 7. Detection and Estimation Theory, 8. EMI/ EMC, 9. ARM Controllers and Embedded C, 10. Internet of Things Lab, 11. Embedded System Design Lab, 12. Seminar.

M. Tech DR25 III & IV Semester Syllabus (Theory & labs)-1. Research Methodology and IPR/Swayam 12-week MOOC course – RM & IPR, 2. Summer Internship / Industrial Training, 3. Comprehensive Viva, 8. Project Work (Dissertation Part – A).

IV Semester Syllabus (Theory & labs)

1,Project Work (Dissertation Part – B)

Other Branches Subjects: 1. Vision Systems and Image Processing.

II. Annexure-B **(Enclosed Annexure -B).**

Agenda Point- 5: Ratification of Course Objectives and Course Outcomes for the proposed subjects.

Resolution: Following detailed discussions, the BoS approved the proposed Course Objectives and Outcomes, incorporating the modifications made to the theory courses and labs outlined in agenda items 3 and 4.

Agenda Point- 6: Finalization of Model Paper. `

Resolution: The BoS members recommended aligning Course Outcomes (COs) with the sequence of exam questions, replacing Knowledge Level (KL) with Bloom's Taxonomy Level (BL), and assigning 4 or 6 marks to select long-answer questions (out of 10). Following confirmation of the COs, BL levels, and marking scheme, the BoS approved the proposed model question papers for external theory course examinations. Annexure-C **(Enclosed Annexure -C).**

Agenda Point 7: Any other item with the permission of the chair.

Resolution: The Chairman of the Board of Studies emphasized the importance of MOOCs and SWAYAM/NPTEL courses for enhancing student skills. He also outlined honors and minor courses, aligned with APSCHE and JNTUK Kakinada guidelines

In conclusion, the Chairman summarized the agenda and resolutions, extended a vote of thanks, and appreciated every member's cooperative effort

Note: All conversations from the BoS meetings are captured on the Zoom platform and kept in the Department's records.

K. Venu Gopal
Chairman, BoS

D.N.R. COLLEGE OF ENGINEERING & TECHNOLOGY
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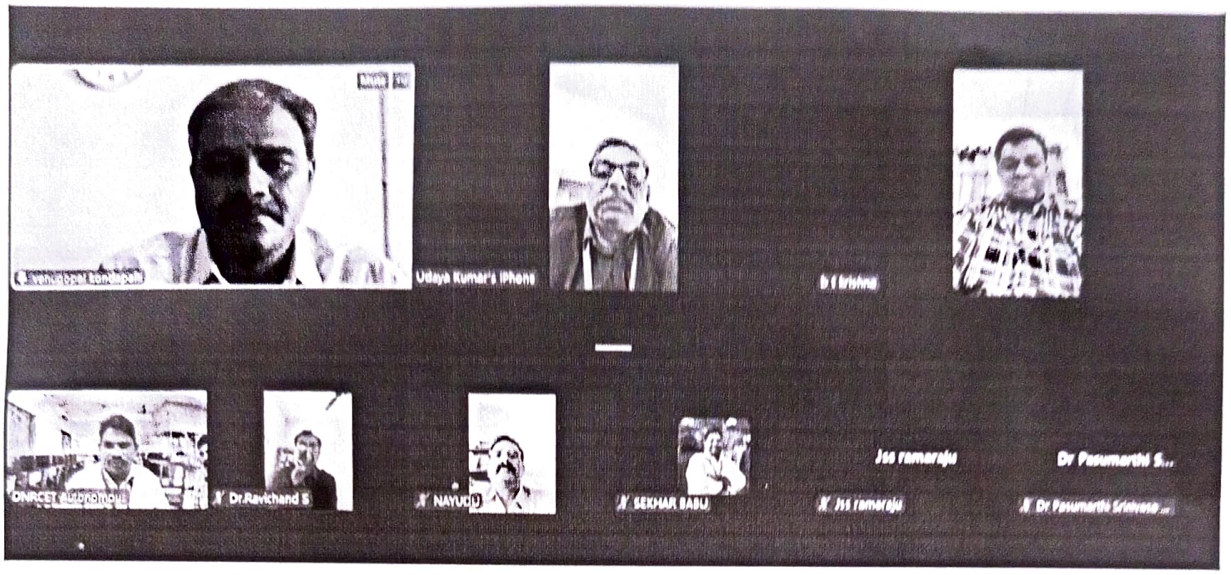
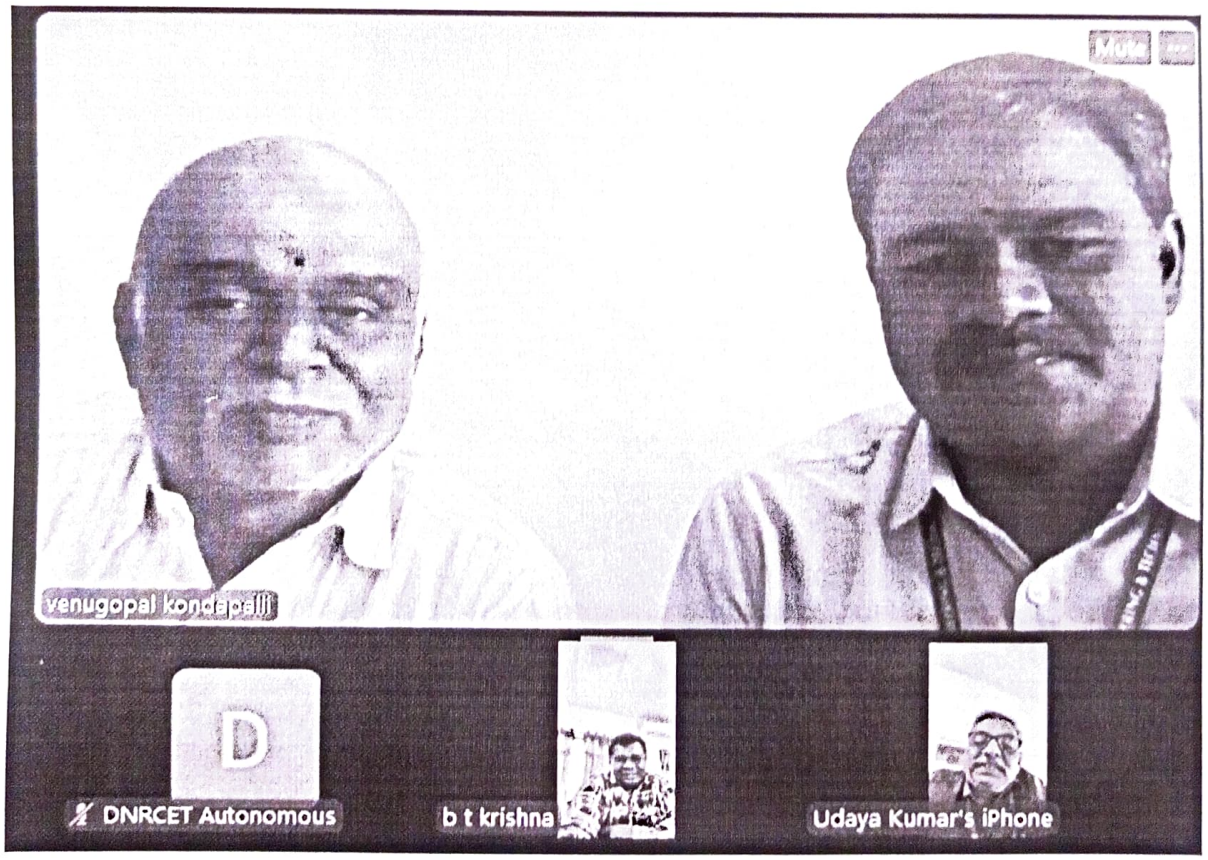
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
09/01/2026.

Ref: DNRCET/ECED/2026-27/BOS-photos/1





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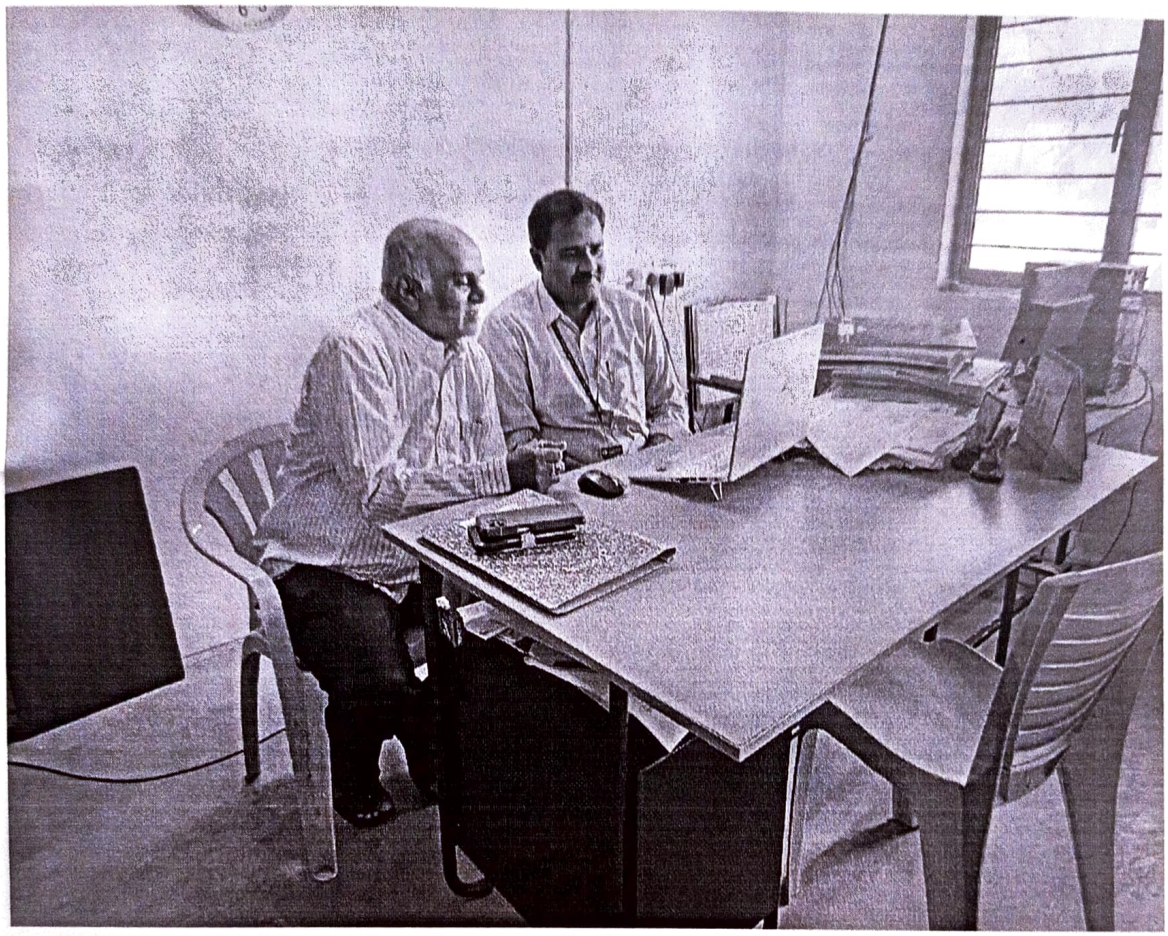

K Venu Gopal
Chairman, BoS

Annexure-B

D.N.R. COLLEGE OF ENGINEERING & TECHNOLOGY
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ACADEMIC REGULATIONS - DR25 FOR M. Tech (REGULAR) DEGREE COURSE

Applicable for the students admitted to M. Tech (Regular) Course from the Academic Year 2025-26 and onwards. The M. Tech Degree of Jawaharlal Nehru Technological University Kakinada shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates (i) in national level qualifying Entrance Test (GATE), (ii) AP PGECET conducted by State Government and (iii) Few Sponsored seats notified by university on the basis of any order of merit as approved by the State Government /University, subject to reservations as laid down by the Government from time to time.

2.0 AWARD OF M. Tech DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech Degree, if he pursues a course of study in not less than two and not more than four academic years. Under any circumstances, permission shall not be given to complete the course work beyond four years.

2.2 **The student shall register for all 80 credits and secure all the 80 credits.**

2.3 The minimum instruction period in each semester is 16 weeks.

3.0 PROGRAMME OF STUDY

The following specializations are offered at present for the M. Tech Programme of study.

M.Tech in

1. Computer Science & Engineering
2. Digital Electronics and Communication Systems
3. Structural Engineering
4. Machine Design

and any other course as approved by AICTE/ University from time to time.

4.0 ATTENDANCE

4.1 Attendance is calculated separately for each course. Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance in each course is 75%. A student shall not be permitted to appear for the Semester End Examinations (SEE), if his/her attendance is less than 75%.

4.2 Condoning of shortage of attendance (between 65% and 75%) up to a maximum of 10% (*considering the days of attendance in sports, games, NSS activities and medical exigencies*) in each course (Theory/Lab/Seminar) is condoned on production of valid Certificates/documents in the stipulated time mentioned here with:

4.2.1 Students who are admitted as in patients for treatment are only eligible to claim condonation of attendance. Such students under medical exigencies need to Produce (a) Doctor Medical Prescription, (ii) Medical bills duly signed by Doctor/Hospital authorities, (c) Diagnosis reports, if any, (d) Discharge summary issued at the time of discharge and any other supporting documents within two week(s) from the date of discharge to the respective institution.

Note: University at any point of time can inform the institution(s) to submit such list/proofs. *Hence, respective institution shall verify and accord condonation privilege scrupulously*.

4.2.2 Students' participation in Sports/Games and NSS activities shall also be permitted for condonation of attendance. In such cases, they need to produce (a) invitation letter from the organizing institute/agency, (ii) participation certificate and any supporting documents within two week(s) from the date of participation to the respective institution

4.3 A prescribed fee per course shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain all the relevant documents along with the request from the students, whose attendance is condoned.

4.4 Shortage of Attendance below 65% in any course shall in no case be condoned.

4.5 A Student, whose shortage of attendance is not condoned in any course(s) (Theory/Lab/Seminar) in any Semester, is considered as '**Detained in that course(s)**, and is not eligible to write Semester End Examination(s) of such Course(s), (in case of Seminar, his/her Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those course(s) in subsequent Semesters, and attend the same as and when offered.

4.6 A student shall put in a minimum required attendance in at least FOUR courses in I semester for promotion to II Semester; and at least FOUR courses in II semester for promotion to III Semester.

Re-admission / re-registration

4.7 A student shall not be permitted to appear for the Semester End Examinations (SEE) in a course unless they meet the prescribed attendance requirements for that course. Such students may take readmission for the course in the subsequent semester when it is offered by paying the prescribed fee, *at least 30 days before the commencement of classwork*. The college must obtain permission from the University by submitting the list of students eligible/applied for readmission before the commencement of classwork

4.8 Students who fail due to **less internal marks (less than 50%)** may register for the course within the maximum permissible duration of the Program.

4.9 In such a case, the candidate must re-register for the course(s) and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon eligibility for writing the end examination in those course(s).

4.10 In a semester, students are permitted to re-register maximum of THREE courses.

4.11 Upon re-registration, the student's previous performance in the respective course(s) will be nullified. Re-registration must be completed by paying the prescribed fee at least 30 days prior to the commencement of classwork. The college is required to obtain approval from the University by submitting a list of eligible and interested students before the start of commencement of classwork.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory courses 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The continuous / internal evaluation shall be made based on the **average** of the marks secured in the two CIE/Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each CIE/midterm examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks. End semester examination is conducted for 60 marks for all FIVE (5) questions (one question from one unit) to be answered (either or).

5.2 For practical courses, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks. The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with breakup marks of Procedure-**15,** Experimentation- **25,** Results-10, Viva-voce-10.

5.3 For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher of the respective college and the second examiner shall be appointed by the University from the panel of examiners submitted by the respective college.

5.8 Students shall undergo mandatory summer internship / industrial training (3 credits) for a minimum of **eight weeks duration** at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before the committee. The Committee comprises of a HoD / Professor of the department and two faculty. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.9 The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. The examination committee will be constituted by the HoD and Professor of the department and two faculty. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.0 EVALUATION OF SEMINAR/INTERNSHIP/DISSERTATION WORK

All the students admitted under these regulations have to mandatorily comply the requirements of (i) Seminar-I, (ii) Seminar-II, (iii) Comprehensive Viva, (iv) Dissertation Part-A and (v) Dissertation Part-B. Out of these, (i) to (iv) are evaluated by internally by Project Review Committee (PRC) and (v) External Evaluation.

6.1 A Project Review Committee (PRC) shall be constituted with Head of the Department and Two other senior faculty members in the department.

6.2 Students are required to appear for Seminar-I and Seminar-II in First and Second semester respectively. They shall present before PRC on the topic of their choice/interest preferably on the courses listed in respective semesters. PRC shall advise the students in advance to select topics which strengthen their Dissertation Part-A and Dissertation Part-B.

6.3 Students shall undergo mandatory summer internship / industrial training (*2 credits*) for a minimum of eight weeks duration at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before PRC. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.4 The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.5 Registration of Dissertation/Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical and duly approved by PRC.

6.6 After satisfying 6.5, student has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval

6.7 If a candidate wishes to change his/her supervisor or topic of the project, he/she can do so with the approval of PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.8 Continuous assessment of Dissertation-Part A and Dissertation-Part B during the Semester(s) will be monitored by PRC. *Dissertation-Part A* will be only internal evaluation by PRC for 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.9 The candidate shall submit a status report to the PRC in two stages, each accompanied by an oral presentation, with a minimum interval of three months between the two.

6.10 The work on the project shall be initiated at the beginning of the III Sem and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis *(Dissertation – Part A & Part B)* only with the approval of PRC not earlier than 40 weeks from the date of registration of the project work.

6.11 Three copies of the project thesis, printed on both sides of the page and certified by the supervisor, shall be submitted to the College/Institute along with the plagiarism report.

6.10 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.11 If the report of the examiner is *not favourable*, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is *not favourable* again, the thesis shall be summarily rejected. The

candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University.

6.12 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination. The Board shall jointly report the candidate's work for a maximum of 100 marks. Corresponding grade will be awarded by the University.

6.13 If the report of the Viva-Voce is unsatisfactory (i.e., < 50 marks), the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.

7.0 Cumulative Grade Point Average (CGPA)

Marks Range (Max – 100)	Letter Grade	Level	Grade Point
≥ 90	S	Outstanding	10
≥80 to <90	A	Excellent	9
≥70 to <80	B	Very Good	8
≥60 to <70	C	Good	7
≥50 to <60	D	Fair	6
<50	F	Fail	3
		Absent	0

Computation of SGPA

- The following procedure is to be adopted to compute the Semester Grade Point Average(SGPA) and Cumulative Grade Point Average (CGPA):
- The **SGPA** is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e
  SGPA (Si) = ∑ (Ci X Gi) / ∑ Ci
- Where Ci is the number of credits of the i^{th} course and Gi is the grade point scored by the student in the i^{th} course.

Computation of CGPA

- The **CGPA** is also calculated in the same manner taking into account all the courses undergone by a student over all the semester of a Programme, i.e.
  CGPA = ∑ (Ci X Si) / ∑ Ci
- Where Si is the SGPA of the i^{th} semester and Ci is the total number of credits in that semester.
- The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
- Equivalent Percentage = (CGPA- 0.5) x 10

8.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	CGPA to be secured	
First Division with Distinction	≥ 7.5 (without supplementary History)	From the CGPA secured from 80 credits
First Class	≥ 6.5	
Second Class	≥ 6.0 to < 6.5	

The secured grade, grade points, status and credits obtained will be shown separately in the memorandum of marks. If a student wants to leave the program / exit after successful completion of first two semesters, he/she will be awarded Post Graduate Diploma in the specialization concerned.

9.0 WITHHOLDING OF RESULTS

If the student is involved in indiscipline/malpractices/court cases, the result of the student will be withheld.

10.0 GENERAL

10.1 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

10.4 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	Both the candidates involved in the malpractice will forefeit their seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.

12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators:

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

Programme Structure

R25 M.Tech Course Structure

M.Tech (XXXX) I – Semester

S. No.	Course Code	Course Title	L	T	P	C
1		Program Core – 1	3	1	0	4
2		Program Core – 2	3	1	0	4
3		Program Core – 3	3	1	0	4
4		Program Elective – I	3	0	0	3
5		Program Elective – II	3	0	0	3
6		Laboratory – 1	0	1	2	2
7		Laboratory – 2	0	1	2	2
8		Seminar-I	0	0	2	1
		TOTAL	**15**	**5**	**6**	**23**

List of Professional Elective Courses in I Semester (Electives – I & II)

S.No.	Course Code	Course Title
1		
2		
3		
4		
5		
6		
7		
8		

@ Minimum 2/3 themes per elective

M.Tech (XXXX) II – Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1		Program Core – 4	3	1	0	4
2		Program Core – 5	3	1	0	4
3		Program Core – 6	3	1	0	4
4		Program Elective – III	3	0	0	3
5		Program Elective - IV	3	0	0	3
6		Laboratory – 3	0	1	2	2
7		Laboratory – 4	0	1	2	2
8		Seminar – II	0	0	2	1
		TOTAL	**15**	**5**	**6**	**23**

List of Professional Elective Courses in II Semester (Electives III & IV)

S.No.	Course Code	Course Title
1		
2		
3		
4		
5		
6		
7		
8		

@ Minimum 2/3 themes per elective

M.Tech (XXXX) - III Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1		Research Methodology and IPR / *Swayam 12 week MOOC course – RM&IPR*	3	0	0	3
2		Summer Internship/ Industrial Training (8-10 weeks)*	-	-	-	3
3		Comprehensive Viva#	-	-	-	2
4		Dissertation Part – A$	-	-	20	10
		TOTAL	**3**	**-**	**20**	**18**

* Student attended during summer / year break and assessment will be done in 3rd Sem.
# Comprehensive viva can be conducted courses completed upto second sem.
$ Dissertation – Part A, internal assessment

M.Tech (XXXX) – IV Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1		Dissertation Part – B%	-	-	32	16
		TOTAL	**-**	**-**	**32**	**16**

% External Assessment

Revised Bloom's Taxonomy Action Verbs

Definitions	I. Remembering	II. Understanding	III. Applying	IV. Analyzing	V. Evaluating	VI. Creating
Bloom's Definition	Exhibit memory of previously learned material by recalling facts, terms, basic concepts, and answers.	Demonstrate understanding of facts and ideas by organizing, comparing, translating, interpreting, giving descriptions, and stating main ideas.	Solve problems to new situations by applying acquired knowledge, facts, techniques and rules in a different way.	Examine and break information into parts by identifying motives or causes. Make inferences and find evidence to support generalizations.	Present and defend opinions by making judgments about information, validity of ideas, or quality of work based on a set of criteria.	Compile information together in a different way by combining elements in a new pattern or proposing alternative solutions.
Verbs	• Choose • Define • Find • How • Label • List • Match • Name • Omit • Recall • Relate • Select • Show • Spell • Tell • What • When • Where • Which • Who • Why	• Classify • Compare • Contrast • Demonstrate • Explain • Extend • Illustrate • Infer • Interpret • Outline • Relate • Rephrase • Show • Summarize • Translate	• Apply • Build • Choose • Construct • Develop • Experiment with • Identify • Interview • Make use of • Model • Organize • Plan • Select • Solve • Utilize	• Analyze • Assume • Categorize • Classify • Compare • Conclusion • Contrast • Discover • Dissect • Distinguish • Divide • Examine • Function • Inference • Inspect • List • Motive • Relationships • Simplify • Survey • Take part in • Test for • Theme	• Agree • Appraise • Assess • Award • Choose • Compare • Conclude • Criteria • Criticize • Decide • Deduct • Defend • Determine • Disprove • Estimate • Evaluate • Explain • Importance • Influence • Interpret • Judge • Justify • Mark • Measure • Opinion • Perceive • Prioritize • Prove • Rate • Recommend • Rule on • Select • Support • Value	• Adapt • Build • Change • Choose • Combine • Compile • Compose • Construct • Create • Delete • Design • Develop • Discuss • Elaborate • Estimate • Formulate • Happen • Imagine • Improve • Invent • Make up • Maximize • Minimize • Modify • Original • Originate • Plan • Predict • Propose • Solution • Solve • Suppose • Test • Theory

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DR25-COURSE STRUCTURE & SYLLABUS
for
M. Tech -ECE

Digital Electronics & Communication Systems (DECS) Programme

(Applicable for batches admitted from 2025-2026)

I Year-I Semester

S. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	D2513800	Mathematical Foundation for Communication Engineering	3	1	0	4
2.	D2513801	Digital System Design	3	1	0	4
3.	D2513802	Wireless Communications & Networks	3	1	0	4
4.	D25138A0 D25138A1 D25138A2	**Elective I** 1. Software Defined Radio 2. Optical Communication & Networks 3. Radio and Navigational Aids	3	0	0	3
5.	D25138B0 D25138B1 D25138B2	**Elective II** 1. FPGA and ASIC Design 2. System Design with RTOS & Embedded LINUX 3. System Design Using Verilog	3	0	0	3
6.	D2513803	Digital System Design Laboratory	0	1	2	2
7.	D2513804	Wireless Communications Laboratory	0	1	2	2
8.	D2513805	Seminar – 1	0	0	2	1
Total Credits			**15**	**5**	**6**	**23**

List of Professionals Elective Courses in I Semester (Electives-I & II)

S. No.	Course Title	Course Code
1	Software Defined Radio	D25138A0
2	Optical Communication & Networks	D25138A1
3	Radio and Navigational Aids	D25138A2
4	FPGA and ASIC Design	D25138B0
5	System Design with RTOS and Embedded LINUX	D25138B1
6	System Design Using Verilog	D25138B2

I Year-II Semester

S. No.	Course Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1.	D3823800	Information Theory and Coding	3	1	0	4
2.	D3823801	IoT & its Communication Protocols	3	1	0	4
3.	D2523802	Embedded System Design	3	1	0	4
4.	D25238A0 D25238A1 D25238A2	**Elective III** 1. Design for Testability 2. MEMS 3. System on Chip Design	3	0	0	3
5.	D25238B0 D25238B1 D25238B2	**Elective IV** 1. Detection and Estimation Theory 2. EMI/ EMC 3. ARM Controllers and Embedded C	3	0	0	3
6.	D2523803	Internet of Things Lab	0	1	2	2
7.	D2523804	Embedded System Design Lab	0	1	2	2
8.	D2523805	Seminar – 2	0	0	2	1
Total Credits			**15**	**5**	**6**	**23**

List of Professionals Elective Courses in II Semester (Electives- III & IV)

S. No	Course Title	Course Code
1	Design for Testability	D25238A0
2	MEMS	D25238A1
3	System on Chip Design	D25238A2
4	Detection and Estimation Theory	D25238B0
5	EMI/ EMC	D25238B1
6	ARM Controllers and Embedded C	D25238B2

II Year-III Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	D2530000	Research Methodology and IPR/ Swayam 12-week MOOC course – RM & IPR	3	0	0	3
2	D2533801	Summer Internship / Industrial Training (8-10 weeks) *	-	-	-	3
3	D2533802	Comprehensive Viva#	-	-	-	2
4	D2533803	Dissertation Part – A$	0	0	20	10
Total			**3**	**0**	**20**	**18**

*Student attended during summer / year break and assessment will be done in 3rd sem.
Comprehensive viva can be conducted courses completed up to second sem.
$ Dissertation – Part A, internal assessment

II Year-IV Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	D2543800	Dissertation Part – B%	--	--	32	16
	Total Credits		--	--	32	**16**

% External Assessment

I Semester	MATHEMATICAL FOUNDATION FOR COMMUNICATION ENGINEERING (D2513800)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. Understand foundational concepts of probability, sampling distributions, estimation, and hypothesis testing for statistical data analysis.
2. Develop analytical skills to handle random processes and Markov chains essential in stochastic modelling and simulation.
3. Acquire computational techniques for solving numerical problems involving interpolation, root finding, ODEs, and eigenvalue problems.
4. Explore mathematical optimization through multivariable calculus, constrained optimization techniques, and numerical methods.
5. Introduce wavelet transform concepts and their application to multi-resolution analysis in data and signal processing.

UNIT- I: Probability and Statistics:

Sampling distributions, Estimation of parameters (point estimation – unbiasedness & minimum variance, basics of interval estimation – confidence interval for mean), Testing of hypotheses (one and two sample tests for mean), Linear regression, Introduction to non-linear regression.

UNIT - II: Stochastic process:

Random processes, Random Walk, Markov process with special emphasis on Markov chain.

UNIT-III: Numerical Analysis:

Introduction to Interpolation formulae [Bessel's & Sterling's], Roots of transcendental equations [Bisection, Regula-Falsi & Newton-Raphson] Solutions of simultaneous non-linear equations [Newton's method], Numerical solution of Ordinary Differential equation [Modified Euler's method, fourth order Runga - Kutta method], Matrix Eigen value and Eigen vector problems.

UNIT- IV: Optimization Technique:

Calculus of several variables, Implicit function theorem, Nature of singular points, Necessary and sufficient conditions for optimization, Constrained Optimization, Lagrange multipliers, Gradient method – steepest descent method.

UNIT- V: Wavelet Transform:
Resolution problems, Multi-resolution analysis, Continuous & discrete wavelet transform

TEXT BOOKS:
1. A. Papoulis and S. Unnikrishnan Pillai, ``Probability, Random Variables and Stochastic Processes," Fourth Edition, McGraw Hill. (Indian Edition is available).
2. Gibert Strang," Linear Algebra and its applications", Thomson Learning Inc, 4th Edition.

REFERENCE BOOKS:
1. H. Stark and J. Woods, 'Probability and Random Processes with Applications to Signal Processing," Third Edition, Pearson Education. (Indian Edition is available).
2. Steven M. Kay, " Intuitive Probability and Random Process using MATLAB", Springer Publications.
3. To dd K Moon, Wynn C. Stirling" Mathematical Methods and Algorithms for Signal Processing, Prentice Hall.

COURSE OUTCOMES
By the end of this course, students will be able to:

1. Apply statistical methods including point estimation, confidence intervals, and hypothesis testing to real-world data scenarios.
2. Model and analyse stochastic systems using random processes, random walks, and Markov chains.
3. Solve engineering and scientific problems using numerical techniques such as Newton-Raphson, interpolation methods, and Runge-Kutta for differential equations.
4. Perform optimization tasks with or without constraints using gradient-based techniques and understand the role of Lagrange multipliers.
5. Use wavelet transforms to analyse signals and data with applications in compression and resolution enhancement.

I Semester	DIGITAL SYSTEM DESIGN (D2513801)	L	T	P	C
		3	1	0	4

Course Objectives:

1. Designing digital circuits, behavior and RTL modelling of digital circuits using Verilog HDL, verifying these Models and synthesizing RTL models to standard cell libraries and FPGAS.
2. Students gain practical experience by designing, modelling, implementing and verifying several digital
3. This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools

UNIT - I:

Introduction to Veril Log HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II:

Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

UNIT -III:

Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators, Design at dataflow level, Parameter and constant usage in dataflow.

UNIT - IV:

Behavioral Modelling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioral Level

UNIT -V:

Verilog Procedural and Control Constructs: Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

TEXTBOOKS:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. Zainalabdien Navabi, Verliog Digital System Design, TMH, 2nd Edition.

REFERENCE BOOKS:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL -Michel D. Ciletti, PHI,2009.

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Understand the syntax, semantics, and simulation principles of Verilog HDL for digital system modelling.
2. Design and implement digital circuits using gate-level modelling and primitive components.
3. Develop dataflow-level models for digital systems using continuous assignments and operators.
4. Apply behavioral modelling techniques to describe complex digital systems using procedural constructs.
5. Utilize control constructs in Verilog to simulate, test, and verify digital designs effectively.

I Semester	WIRELESS COMMUNICATIONS & NETWORKS (D2513802)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. To introduce the cellular system design concepts including frequency reuse, interference management, and handoff strategies.
2. To understand large-scale radio wave propagation models and their impact on wireless system performance.
3. To study small-scale fading, multipath propagation effects, and statistical models for channel behavior.
4. To explore equalization and diversity techniques for improving signal quality in wireless environments.
5. To provide an overview of wireless networks and standards such as IEEE 802.11, IEEE 802.16, and wireless PANs.

UNIT-I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Trunking and Grade of Service.

UNIT-II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, Basic Propagation Mechanisms, **Reflection**: Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, **Diffraction**: Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife- edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models- Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT -III

Mobile Radio Propagation: Small–Scale Fading and Multipath Small Scale Multipath propagation- Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT-IV

Equalization and Diversity Introduction, Fundamentals of Equalization, Training a Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non-linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity -Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization
Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT-V

Wireless Networks Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11, IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – GottapuSasi bhushanaRao, Pearson Education, 2012.

REFERENCE BOOKS:

1. Principles of Wireless Networks – KavehPahLaven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – KamiloFeher, 1999, PHI. Wireless Communication and Networking – William Stalling

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Understand cellular system design concepts including frequency reuse, interference management, and handoff strategies.
2. Analyse large-scale radio propagation models and apply them to outdoor and indoor wireless environments.
3. Evaluate small-scale fading effects and multipath propagation using statistical and empirical models.
4. Apply equalization and diversity techniques to improve wireless communication performance under varying channel conditions.
5. Demonstrate knowledge of wireless network standards, architectures, and protocols including IEEE 802.11 and 802.16.

I Semester	SOFTWARE DEFINED RADIO (D25138A0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Introduce the evolution of radio communication systems and the fundamental concepts, architectures, and design principles of Software Defined Radio (SDR).
2. Understand the implementation challenges in RF front-end systems, including dynamic range, receiver topologies, and performance-affecting factors.
3. Explore digital signal generation techniques, particularly direct digital synthesis (DDS), and analyse related spurious signal behaviors.
4. Introduce multirate signal processing methods such as sample rate conversion, polyphase filters, and timing recovery in digital receivers.
5. Study analog-to-digital and digital-to-analog conversion techniques and methods for improving data converter performance in SDR systems.

UNIT- I:

Introduction to Software radio concepts: Introduction, need, characteristics, benefits and design principles of Software Radios. Traditional radio implemented in hardware (first generations of 2G cell phones), Software controlled radio (SCR), Software defined radio (SDR), Ideal software radio (ISR), Ultimate software radio (USR)

UNIT- II:

Radio frequency implementation issues: The purpose of RF Front-End, Dynamic range, RF Receiver Front-End Topologies, Enhanced Flexibility of the RF Chain with Software Radios, Importance of Components to Overall performance, Transmitter Architecture and their issues, Noise and Distortion in RF Chain.

UNIT -III:

Digital generation of signals: Introduction, Comparison of Direct Digital Synthesis with Analog Signal Synthesis, Approaches to Direct Digital Synthesis, Analysis of Spurious Signals, Spurious components due to Periodic Jitter.

UNIT-IV:

Multirate Signal Processing: Introduction, Sample Rate Conversion Principles, Polyphase Filters, Digital Filter Banks, Timing Recovery in Digital receivers Using Multirate Digital Filters.

UNIT- V:

A/D & D/A Conversion: Introduction, Parameters of Ideal Data Converters, Parameters of Practical data Converters, Techniques to improve Data Converter performance, JTRS.

TEXT BOOKS:

1. Jeffery H. Reed, "Software Radio, (A modern approach to radio engineering)", PHI PTR, 2002
2. John J. Rouphael, "RF and Digital Signal Processing for Software Defined Radio" Elsevier, Newness Publications.

REFERENCE BOOKS:

1. C. Richard Johnson, Jr., and William A. Sethares, Telecommunication Breakdown, Prentice Hall, ISBN 0-13-143047-5, 2004
2. Software Defined Radio: Theory and Practice by John M. Reyland (Artech House, 2023)

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Know the fundamentals of Software Radios, their evolution from traditional radios, and various levels including SCR, SDR, ISR, and USR.
2. Analyse RF front-end architectures, dynamic range requirements, and the role of RF Components in system performance for Software Radio implementation.
3. Explain and compare different signal generation techniques including direct digital synthesis, and analyse sources of spurious components and jitter effects.
4. Apply multi-rate signal processing techniques such as sample rate conversion, polyphase Filtering, and digital filter banks in software radio systems.
5. Evaluate the performance of A/D and D/A converters in practical systems, and describe Methods to improve conversion performance, including relevance to JTRS

I Semester	OPTICAL COMMUNICATION & NETWORKS (D25138A1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Introduce the fundamentals of optical fiber communication, including transmission link components, light propagation, and fiber structures.
2. Understand the principles and performance of optical sources and detectors used in optical communication systems.
3. Explain the structure and function of optical communication systems, including digital systems and modern high-speed links.
4. Familiarize students with components and technologies used in fiber optic networks and their architectures.
5. Explore coherent communication systems, detection techniques, and the role of demodulation and noise management in optical receivers.

UNIT- I:

Overview of optical fiber communications: Elements of an optical fiber transmission link. Optical Fibers: structures, wave guiding, Nature of light, Basic optical laws and definitions, optical fiber modes and configurations (Fiber types, Rays and modes, step index and graded index fibers) mode theory of circular waveguides. (Qualitative Treatment) Fabrication, cabling and installation: Fabrication, fiber optic cables, Installation- placing the cable.

UNIT -II:

Optical sources: LEDs, structures, quantum efficiency, modulation capability, Laser diodes: Laser diodes and threshold conditions, external quantum efficiency resonant frequencies, **Optical Detectors**: Physical principles of photodiodes (pin Photodiode, avalanche, photo diode) comparison of photo detectors, noise in detectors.

UNIT -III:

Optical Communication Systems: Block diagrams of optical communication systems, direct intensity modulation, digital communication systems, Laser semiconductor transmitter, Generations of optical fiber link, description of 8 Mb/s optical fiber communication link, description of 2.5 Gb/s optical fiber communication link.

UNIT -IV:

Components of fiber optic Networks: Overview of fiber optic networks, Trans receiver, semiconductors optical amplifiers, couplers/splicer's, wavelength division multiplexers and demultiplexers, filters, isolators and optical switches. **Fiber Optic Networks**: Basic networks, SONET/SDIT, Broad cast and select WDM Networks, wavelength routed networks, optical CDMA Nonlinear effects on network performance.

UNIT- V:

Coherent Systems: Coherent receiver, Homodyne and heterodyne detection, noise in coherent receiver, polarization control, Homodyne receiver, Reusability and laser line-width, heterodyne receiver, synchronous, Asynchronous and self-synchronous demodulation, phase diversity receivers.

TEXT BOOKS:

1. Optical fiber communications – Gerd Keiser, 3 rd Ed. MGH.
2. Fiber Optic Communication Technology – Djafar K. Mynbaev and Lowell L. Scheiner,
3. Optoelectronic devices and systems – S.C. Gupta, PHI, 2005.

REFERENCE BOOKS:

1. Fiber Optics Communications – Harold Kolimbiris (Pearson Education Asia)
2. Optical Fiber Communications and its applications – S.C. Gupta (PHI) 2004.

COURSE OUTCOMES:

Upon completion of the course students will be able to :

1. Explain the fundamental principles of optical fiber communication including Wave guiding, fiber types, and mode theory of circular waveguides.
2. Compare and analyze various optical sources (LEDs, laser diodes) and detectors (PIN, APD) in terms of efficiency, modulation capability, and noise performance.
3. Design and interpret the block diagrams of optical communication systems and explain the working of digital systems including 8 Mb/s and 2.5 Gb/s optical links.
4. Evaluate different fiber optic network components such as transceivers, amplifiers, WDM Systems.
5. Demonstrate understanding of coherent optical systems including homodyne/heterodyne detection, polarization effects, and noise handling in coherent receivers.

I Semester	RADIO AND NAVIGATIONAL AIDS (D25138A2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Understand the principles and configurations of radio positioning systems and factors affecting positioning accuracy.
2. Explore terrestrial radio navigation systems including LORAN, ILS, and indoor/urban positioning technologies.
3. Introduce fundamental navigation concepts such as position fixing, dead reckoning, and integrated navigation systems.
4. Study advanced satellite navigation techniques including Differential GNSS and carrier-phase positioning.
5. Examine inertial navigation systems and their equations, alignment methods, and error propagation models.

UNIT- I: Principles of Radio Positioning: Radio Positioning Configurations and Methods, Positioning Signals, User Equipment, Propagation, Error Sources, and Positioning Accuracy. Terrestrial Radio Navigation: Point-Source Systems, Loran, Instrument Landing System, Urban and Indoor Positioning, Relative Navigation, Tracking, Sonar Transponders.

UNIT- II: Introduction to Navigation: What Is Navigation, Position Fixing, Dead Reckoning, Inertial Navigation, Radio and Satellite Navigation, Terrestrial Radio Navigation, Satellite Navigation, Feature Matching, The Complete Navigation System.

UNIT- III: Advanced Satellite Navigation: Differential GNSS, Carrier-Phase Positioning and Attitude, Poor Signal-to-Noise Environments, Multipath Mitigation, Signal Monitoring, Semi Codeless Tracking.

UNIT- IV: Inertial Navigation: Inertial-Frame Navigation Equations, Earth-Frame Navigation Equations, Local-Navigation-Frame Navigation Equations, Navigation Equations Precision, Initialization and Alignment, INS Error Propagation, Platform INS, Horizontal-Plane Inertial Navigation.

UNIT- V: Satellite Navigation & GNSS Systems: Fundamentals: GPS, GLONASS, Galileo, Beidou, IRNSS, signal structure, measurement errors (ionospheric/tropospheric/multipath), Dilution of Precision (GDOP, PDOP), ephemeris, clock/correction errors, Differential GNSS, WAAS, integrity monitoring, carrier-phase techniques.

TEXT BOOKS:

1. G S RAO, Global Navigation Satellite Systems, McGraw-Hill Publications, New Delhi, 2010.
2. Principles of GNSS, Inertial, and Multisensor Integrated Navigation Systems, Paul D. Groves Artech House, 2008 and 2013 Second Edition.
3. 2. B. Hofmann Wollenhof, H. Lichtenegger, and J. Collins, "GPS Theory and Practice", Springer Wien, New York, 2000.

REFERENCE BOOKS:

1. Pratap Misra and Per Enge, "Global Positioning System Signals, Measurements, and Performance," Ganga-Jamuna Press, Massachusetts, 2001.
2. Ahmed El-Rabbany, "Introduction to GPS," Artech House, Boston, 2002.
3. Bradford W. Parkinson and James J. Spilker, "Global Positioning System: Theory and Applications," Volume II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Explain the principles, configurations, and error sources of terrestrial and radio positioning systems.
2. Apply various navigation methods to determine position and trajectory.
3. Analyse advanced satellite navigation techniques for accuracy enhancement.
4. Evaluate inertial navigation equations, alignment methods, and error propagation.
5. Integrate GNSS systems with error correction techniques for reliable navigation solutions.

I Semester	FPGA and ASIC DESIGN (D25138B0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the evolution, design flow, and applications of FPGAs and PLDs.
2. To study various FPGA/CPLD programming technologies and commercially available devices.
3. To understand the internal architecture and building blocks of FPGAs/CPLDs and their impact on performance.
4. To explore routing architectures and strategies used in different FPGA types.
5. To analyse architectural elements and apply FPGA technology in real-world case studies.

UNIT-I:

INTRODUCTION TO FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.

DESIGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter

UNIT-II:

FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Axtel's FPGA, Altera's FPGA/CPLD.

UNIT-III:

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT-IV:

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures

UNIT-V:

FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA CASE STUDY – Applications using Kintex-7, Virtex-7, Artix-7.

TEXT BOOKS:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
2. VLSI Design: A Practical Guide for FPGA and ASIC Implementations by Vikram A. Chandrasetty (Springer Briefs, 2011).

REFERENCE BOOKS:

1. Data sheets of Artix-7, Kintex-7, Virtex-7
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

COURSE OUTCOMES:

Upon completion of the course students will be able to :

1. Explain the evolution, design flow, and practical applications of FPGAs and PLDs.
2. Compare different FPGA/CPLD devices and their programming technologies.
3. Analyse the architecture of logic blocks, routing structures, and I/O blocks in FPGAs.
4. Apply routing techniques to various FPGA architectures for optimized performance.
5. Demonstrate FPGA design implementation using case studies on Kintex-7, Virtex-7, and Artix-7.

I Semester	SYSTEM DESIGN WITH RTOS & EMBEDDED LINUX (D25138B1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the key concepts of Real-Time Operating Systems and task management fundamentals.
2. To explore synchronization and communication mechanisms used in real-time systems.
3. To understand the role of exceptions, interrupts, and timer services in RTOS environments.
4. To provide hands-on experience with Linux kernels and shell scripting for embedded applications.
5. To analyse embedded Linux architecture and understand the process of application porting and driver integration.

UNIT- I: Introduction to RTOS and Task Management

Introduction to Real-Time Operating Systems (RTOS): Key characteristics, scheduler, kernel objects and services, system calls, static and dynamic libraries, cross tool chains, Task management: Defining tasks, task states, scheduling, task operations, synchronization, communication, concurrency.

UNIT- II: Synchronization, Communication, and I/O Systems

Semaphores: Operations, use cases, Message Queues: Types, operations, use cases (including pipes, event registers, signals, condition variables), I/O Subsystems: I/O concepts, subsystems, Synchronization and Communication: Resource synchronization methods, critical section, design patterns, priority inversion, common design problems (deadlocks, priority inversion).

UNIT- III: Exceptions, Interrupts, and Timer Services

Exceptions and Interrupts: Definitions, applications, spurious interrupts, Timer Services: Real-time clocks, system clocks, programmable interval timers, timer interrupt service routines.

UNIT -IV: Linux Kernel and Shell Scripting

Introduction to Linux Kernels: Linux basics, GNU utilities, distributions, access methods (CLI, graphical terminal emulators), Bash Shell Commands: Navigation, file handling, system monitoring, environment variables, user-defined variables, Shell Scripting: Script creation, control structures (if-else, loops, case commands), output redirection, practical examples, handling signals, background scripts, basic script functions, alternative shells (dash, zsh).

UNIT -V: Embedded Linux Architecture and Application Porting

Embedded Linux Architecture: Kernel architecture, memory manager, scheduler, file system, I/O and networking subsystems, IPC, user space, startup sequence, Board Support Package: Embedded storage (MTD), embedded file system, embedded device drivers (communication kernel modules), Porting Applications: Real-time Linux, hard real-time programming, building and debugging (bootloaders, kernel, root file system, device tree).

TEXT BOOKS:

1. Qing Li, Caroline Yao (2020), "Real-Time Concepts for Embedded Systems", CMP Books.

2. Chris Simmonds, "Mastering Embedded Linux Programming" - Second Edition, PACKT Publications Limited.

REFERENCE BOOKS:

1. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates.

2. Mastering Embedded Linux Programming (3rd Edition) by Frank Vasquez & Chris Simmonds.

COURSE OUTCOMES:

After completing the course, students will be able to:

1. Describe RTOS features, kernel components, and manage task scheduling and synchronization.
2. Implement inter-task communication using semaphores, message queues, and handle I/O operations effectively.
3. Analyse the behaviour of exceptions, interrupts, and use timer services in real-time systems.
4. Use Linux shell commands and scripts to perform system-level operations and automation tasks.
5. Demonstrate understanding of embedded Linux internals and port applications with BSP and device drivers.

I Semester	SYSTEMS DESIGN USING VERILOG (D25138B2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Designing digital circuits, behaviour and RTL modelling of digital circuits using verilog HDL, verifying these Models and synthesizing RTL models to standard cell libraries and FPGAS.
2. Students gain practical experience by designing, modelling, implementing and verifying several digital
3. This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools.

UNIT - I: Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II: Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

UNIT -III: Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators, Design at dataflow level, Parameter and constant usage in dataflow.

UNIT - IV: Behavioural Modelling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioural Level

UNIT -V: Verilog Procedural and Control Constructs: Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

TEXT BOOKS:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. Zainalabdien Navabi, Verliog Digital System Design, TMH, 2nd Edition.

REFERENCE BOOKS:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL -Michel D. Ciletti, PHI,2009.

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Describe Verilog hardware description, languages (HDL).
2. Design digital circuits.
3. Write Behavioral models of digital circuits.
4. Write Register Transfer Level (RTL) models of Digital Circuits.
5. Verify Behavioral and RTL models.

I Semester	DIGITAL SYSTEM DESIGN LABORATORY (D2513803)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To introduce algorithms for efficient combinational and sequential logic design such as CAMP-I, CAMP-II, and Kohavi.
2. To familiarize students with programmable logic array (PLA) design, minimization, and folding techniques.
3. To develop skills in the design and implementation of ROM and control logic units.
4. To enable practical experience in digital system implementation using FPGA platforms.
5. To understand and experiment with error detection/correction and finite state machine design concepts.

Systems Design experiments:

- The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
- Consider the suitable switching function and data to implement the required logic if required.

A student must do at least 10 Experiments.

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm)
5. PLA folding algorithm (COMPACT algorithm)
6. ROM design.
7. Control unit and data processor logic design
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Apply CAMP-I and CAMP-II algorithms to determine essential, secondary, and spurious prime implicants.
2. Implement PLA minimization and folding using IISc and COMPACT algorithms respectively.
3. Design **and** realize ROM-based systems and control/data path logic circuits.
4. Develop digital systems using FPGA tools and platforms for real-time applications.
5. Perform logic minimization using Kohavi's algorithm and **analyze** error-correcting codes through Hamming experiments.

I Semester	WIRELESS COMMUNICATIONS LABORATORY (D2513804)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To understand and analyse digital communication techniques including error detection and correction.
2. To provide hands-on experience in spread spectrum systems, convolutional coding, and decoding.
3. To apply signal processing techniques using transforms, filtering, and DSP hardware platforms.
4. To explore image processing operations and study their effects on digital images.
5. To study and experiment with optical fiber communication, mobile phone trainers, CDMA, and ISDN systems.

PART A: List of Experiments :(Minimum of Ten Experiments must be performed)

1.Measurement of Bit Error Rate using Binary Data.
2. Verification of minimum distance in Hamming code
3.Determination of output of Convolution Encoder for a given sequence.
4.Determination of output of Convolution Decoder for a given sequence.
5.Efficiency of DS Spread- Spectrum Technique
6. Simulation of Frequency Hopping (FH) system
7. Effect of Sampling and Quantization of Digital Image
8. Verification of Various Transforms (FT / DCT/ Walsh / Hadamard) on a given Image (Finding Transform and Inverse Transform)
9. Point, Line and Edge detection techniques using derivative operators.
10.Implementation of FIR filter using DSP Trainer Kit (C-Code/ Assembly code)
11. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code).
12. Determination of Losses in Optical Fiber.
13. Observing the Waveforms at various test points of a mobile phone using Mobile Phone Trainer.
14. Study of Direct Sequence Spread Spectrum Modulation & Demodulation using CDMA-DSSBER Trainer.
15. Study of ISDN Training System with Protocol Analyzer.
16. Characteristics of LASER Diode.

PART B: Equipment required for Laboratory Software:

1. MATLAB along with Simulink Licensed simulation software tool with communication and Signal processing Toolbox.
2. Computer Systems with required specifications

Hardware:

1. Hardware kits for verification of BER
2. Hardware kits of Convolution encoders, Hamming encoders.
3. Frequency spectrum
4. Mobile Phone Trainer
5. DSP Trainer Kit
6. CDMA-DSS-BER Trainer
7. ISDN Training System with Protocol Analyzer
8. Optical fiber Transmitter and receiver kit along with different lengths of cables

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Measure bit error rates and verify error correction capabilities using Hamming codes.
2. Simulate and analyse convolutional encoder/decoder systems and spread spectrum techniques.
3. Implement and evaluate digital signal processing algorithms (FIR/IIR filters) on DSP trainer kits.
4. Apply transforms (FT, DCT, Walsh, Hadamard) and perform edge/line detection in digital images.
5. Experiment with optical fiber characteristics, mobile phone trainer systems, and CDMA/ISDN technologies.

I Semester	SEMINAR – I (D2513805)	L	T	P	C
		0	0	2	1

For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

II Semester	INFORMATION THEORY AND CODING (D2523800)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. Introduce core concepts of information theory including entropy and mutual information.
2. Teach lossless source coding algorithms like Huffman, Arithmetic, and LZW.
3. Explain channel capacity and its evaluation for various communication channels.
4. Explore the fundamentals of video and speech coding techniques.
5. Provide knowledge of error control coding for reliable data transmission.

UNIT-I: Introduction

Information Source, Symbols, and Entropy, Mutual information, information Measures for Continuous Random Variable, Joint and Conditional Entropy, Relative Entropy, Applications Based on information Theoretic Approach.

UNIT-II: Source coding

Source Coding Theorem, Kraft inequality, Shannon-Fano Codes, Huffman Codes, Run Length Code, Arithmetic Codes, Lempel-Ziv-Welch Algorithm, Universal Source Codes, Prefix Codes, Variable Length Codes, Uniquely Decodable Codes, instantaneous Codes, Shannon's Theorem, Shannon Fano Encoding Algorithm, Shannon's Noiseless Coding Theorem, Shannon's Noisy Coding Theorem.

UNIT-III: Communication channel

Channel and its Capacity, Continuous and Gaussian Channels, Discrete Memory-Less Channels, Symmetric Channel, Binary Erasure Channel, Estimation of Channel Capacity, Noiseless Channel, Channel Efficiency, Shannon's Theorem on Channel Capacity, Mimo Channels, Channel Capacity with Feedback.

UNIT-IV: Video and speech coding

Video Coding Basics, Quantization, Symbol Encoding, Intraframe Coding, Predictive Coding, Transform Coding, Subband Coding, Vector Quantization, Interframe Coding, Motion Compensated Coding, Image Compression, Jpeg, LZ78 Compression, Dictionary Based Compression, Statistical Modelling, Speech Coding, Psycho-Acousting Modelling, Time Frequency Mapping Quantization, Variable Length Coding, Multichannel Correlation and Irrelevancy, Long Term Correlation, Pre-Echo Control, Bit Allocation.

UNIT-V: Error control coding

Overview of Field, Group, Galois Field, Types of Codes, Hamming Weight, Minimum Distance Based Codes, Error Detection and Error Correction Theorems, Maximum Likelihood Decoder, Map Decoder, Linear Block Codes and Their Properties, Equivalent Codes, Generator Matrix and Parity Check Matrix, Systematic Codes, Cyclic Codes, Convolution Codes and Viterbi Decoding Algorithm, Iterative Decoding, Turbo Codes and Low Density-Parity-Check Codes, Asymptotic Equipartition Property, Bch Codes, Generator Polynomials, Decoding of Bch Codes, Reed Solomon Codes, Trellis Codes, Space Time Coding.

TEXT BOOKS:

1. T.M. Cover and J.A. Thomas, Elements of Information Theory, John Wiley & Sons.
2. Todd K. Moon, Error Correction coding, John Wiley, 2005.

REFERENCE BOOKS:

1. Shu lin/ Daniel J.Costello Jr., Error Control Coding, Prentice Hall series in computer applications in electrical engineering series (2/e) 2005.
2. Ranjan Bose, Information Theory, coding and cryptography (2/e), McGraw Hill

COURSE OUTCOMES:

1. Understand and compute entropy, mutual information, and related measures.
2. Apply and analyse source coding algorithms for efficient data compression.
3. Evaluate channel capacity and efficiency in communication systems.
4. Implement and compare video/speech coding and multimedia compression techniques.
5. Design and analyse error control codes for error detection and correction

II Semester	IOT AND ITS COMMUNICATION PROTOCOLS (D2523801)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. Introduce the core architecture and technologies of IoT**,** including devices, gateways, networking, data management, and services.
2. Familiarize students with IoT reference architectures, views, and the design constraints encountered in real-world implementations.
3. Understand data link and network layer protocols that support communication in IoT systems, including both traditional and IoT-specific protocols.
4. Explore transport and session layer protocols essential for reliable and efficient data transfer in IoT communication models.
5. Explain service layer and security protocols used in IoT systems, emphasizing interoperability and secure communication.

UNIT-I

Introduction: IoT architecture outline, standards - IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service (XaaS), M2M and IoT Analytics

UNIT-II

IoT Reference Architecture: Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints-Introduction, Technical Design constraints

UNIT-III

IoT Data Link Layer & Network Layer Protocols: PHY/MAC Layer (3GPP MTC, IEEE 802.11, IEEE 802.15), Wireless HART, Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH7 - Network Layer-IPv4, IPv6, 6LoWPAN, 6TiSCH, ND, DHCP, ICMP, RPL, CORPL, CARP

UNIT -IV

IoT Transport & Session Layer Protocols: Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, CoAP, XMPP, AMQP, MQTT

UNIT -V

IoT Service Layer Protocols & Security Protocols: Service Layer -oneM2M, ETSI M2M, OMA, BBF – Security in IoT Protocols – MAC802.15.4 , 6LoWPAN, RPL, Application Layer.

TEXT BOOKS:

1 Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications", ISBN: 978-1-118-47347-4, Willy Publications ,2016.

2 Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Aves and, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2015.

REFERENCE BOOKS

1. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642 19156-5 e-ISBN 978-3-642-19157-2, Springer, 2016.
2. N. Ida, Sensors, Actuators and Their Interfaces, Scitech Publishers, 2014.

COURSE OUTCOMES:

1.Understand the fundamental components and architecture of IoT systems.
2. Interpret and apply various IoT reference architectural views.
3. Analyse datalink and network layer protocols used in IoT communication
4. Evaluate transport and session layer protocols for their suitability in IoT applications
5. Assess IoT service layer and security protocols to ensure interoperability and secure communication

II Semester	EMBEDDED SYSTEM DESIGN (D2523802)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. To introduce the fundamentals, classification, and characteristics of embedded systems.
2. To explore the core components of embedded systems including processors, memory, and interfaces.
3. To understand embedded firmware components and design approaches.
4. To study ARM processor architecture, instruction sets, and programming model.
5. To provide practical exposure to Raspberry Pi programming, communication protocols, and sensor interfacing.

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT- II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

ARM: ARM design philosophy, data flow model and core architecture, registers, program status register, instruction pipeline, interrupts and vector table, operating modes and ARM processor families. Instruction Sets: Data processing instructions, addressing modes, branch, load, store instructions, PSR instructions, and conditional instructions.

UNIT -V

Raspberry Pi: Raspberry Pi board and its processor, Programming the Raspberry Pi using Python, Communication facilities on Raspberry Pi (I2C, SPI, UART), Interfacing of sensors and actuators.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.
2. A. N. Sloss, D. Symes, and C. Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Elsevier, 2008.
3. S. Monk, “Programming the Raspberry Pi” McGraw-Hill Education, 2013.

REFERENCE BOOKS:

1. Steave Furber, “ARM system-on-chip architecture”, Addison Wesley, 2000.
2. Embedded Systems - Raj Kamal, TMH.
3. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Describe the structure, classification, and purpose of embedded systems and their quality attributes.
2. Analyse embedded system components such as processors, memory types, sensors, actuators, and interfaces.
3. Explain embedded firmware building blocks and apply suitable design approaches.
4. Demonstrate knowledge of ARM architecture and instruction sets relevant to embedded programming.
5. Develop simple embedded applications using Raspberry Pi and interface sensors and communication peripherals.

II Semester	DESIGN FOR TESTABILITY (D25238A0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamental concepts, types, and philosophies of VLSI testing.
2. To familiarise fault models and apply logic/fault simulation techniques for test evaluation.
3. To study testability measures and design-for-test (DFT) techniques including scan design.
4. To explore Built-In Self-Test (BIST) strategies and their application in digital systems.
5. To learn the boundary scan architecture and standards used in board-level testing.

UNIT-I: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III: Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V: Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

2. VLSI Test Principles and Architectures: Design for Testability" – L.-T. Wang, C.-W. Wu, X. Wen

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

COURSE OUTCOMES:

1. Explain the role of testing in VLSI systems and differentiate between fault models and testing types.
2. Apply simulation algorithms for design verification and fault analysis in digital circuits.
3. Evaluate testability using measures like SCOAP and design scan-based test structures.
4. Design and implement BIST strategies for logic and memory testing.
5. Demonstrate understanding of boundary scan standards and describe systems using BSDL.

II Semester	MEMS (D25238A1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamentals, materials, and applications of MEMS and smart systems.
2. To explore various types of micro-sensors, actuators, and smart material-based systems.
3. To study micro-fabrication techniques including deposition, lithography, and micromachining.
4. To understand the mechanical modelling of microstructures such as beams, bars, and multilayer elements.
5. To apply numerical analysis techniques like Finite Element Method (FEM) for modelling MEMS structures.

UNIT-I

Introduction to MEMS: Microsystems versus MEMS, Micro fabrication, Smart Materials, Structures and Systems, Integrated Microsystems, Applications of Smart Materials and Microsystems

UNIT-II

Micro Sensors, Actuators, Systems and Smart Materials: Silicon Capacitive Accelerometer, Piezo-resistive Pressure Sensor, Conductometric Gas Sensor, An Electrostatic Comb-Drive, A Magnetic Micro relay, Portable Blood Analyzer, Piezoelectric Inkjet Print Head, Micro-mirror Array for Video Projection Smart Materials and Systems

UNIT -III

Micro Fabrication Technique: Silicon as a Material for Micromachining, Thin-Film Deposition, Lithography, Etching, Silicon Micromachining Specialized Materials for Microsystems, Advanced Processes for Micro fabrication

UNIT-IV

Modeling Of Solids in Microsystems: The Simplest Deformable Element: A Bar, Transversely Deformable Element: A beam, Energy Methods for Elastic Bodies, Heterogeneous Layered Beams, Bimorph Effect, Residual Stresses and Stress Gradients, Poisson Effect and the Anticlastic Curvature of Beams, Torsion of Beams and Shear Stresses, Dealing with Large Displacements, In-Plane Stresses

UNIT-V

Finite Element Method: Need for Numerical Methods for Solution of Equations - Variational Principles, Finite Element Method, Finite Element Model for Structures with Piezoelectric Sensors and Actuators, Analysis of a Piezoelectric Bimorph Cantilever Beam

TEXT BOOKS:

1. Fundamentals of Microfabrication — *Marc J. Madou* (CRC Press, 1997/2002).
2. An Introduction to Microelectromechanical Systems Engineering — N. Maluf (Artech House, 1999).

REFERENCE BOOKS:

1. Micro and Smart Systems by G.K. Ananthasuresh, K.J. Vinoy, S.Gopalakrishnan, K.N.Bhat, V.K.Aatre: Wiley, India (2016).

2. Smart Material Systems and MEMS: Design and Development Methodologies: Vijay K., 2017
   The MEMS Handbook: Edited by Mohamed Gad-el-Hak, University of NotreDame, CRC Press LLC, 2015

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Describe the basic concepts of MEMS, microfabrication, and smart materials.
2. Identify and explain the working principles of micro-sensors, actuators, and MEMS devices.
3. Demonstrate knowledge of various micro-fabrication processes used in MEMS manufacturing.
4. Analyse mechanical behaviour of MEMS structures using energy methods and elasticity concepts.
5. Apply FEM techniques for modelling and simulation of MEMS devices with piezoelectric elements.

II Semester	SYSTEM ON CHIP DESIGN (D25238A2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamentals of SoC architecture, components, and design methodologies.
2. To understand hardware-software co-design concepts including partitioning, scheduling, and hardware acceleration.
3. To explore virtual prototyping, high-level synthesis, and system-level design methodologies.
4. To examine SoC interconnection structures and protocols like AMBA AXI and Network-on-Chip (NoC).
5. To analyse performance and power at the system level using simulation platforms and case studies.

UNIT-I: SoC Design Approach: Basics of Chips and SoC ICs, SoC Design: SoC CPU/IP Cores, Co-processor, Cache, DRAM Controller, SoC Synthesis, Static Timing Analysis (STA), Design for Testability, Verification, Physical Design.

UNIT-II:
Hardware-Software Co-Synthesis: Partitioning, Cycle Time, Die Area and Cost, Power, Area-Time-Power Trade-offs and Chip Reliability, Real-Time Scheduling, Hardware Acceleration.

UNIT-III: Virtual Prototyping and High-Level Synthesis (HLS): Mapping High-Level Language Applications to Hardware, Transaction-Level Modeling and Electronic System-Level Languages, Hardware Accelerators, Media Instructions, Coprocessors, System-Level Design Methodology, High-Level Synthesis (C-to-RTL), Hardware Synthesis and Architecture Techniques, Source-Level Optimizations.

UNIT-IV: SoC Interconnection Structures: Bus-Based Interconnection, Bus Protocols: AMBA AXI Bus, AXI4-Stream, IBM Core Connect, Avalon. Interconnection Structures, Network on Chip (NoC) Interconnection and NoC Systems, IP Interfacing.

UNIT-V: Performance/Power Analysis of SoCs: System-Level Modeling and Integration, Simulation Platform for Performance Analysis of SoC/MPSoC, Use Cases and Examples.

TEXT BOOKS:

1. Veena Chakravarthi, A Practical Approach to VLSI System on Chip (SoC) Design – A Comprehensive Guide, Springer, 2020
2. S. Pasricha and N. Dutt, On-Chip Communication Architectures: System on Chip Interconnect, Morgan Kaufmann–Elsevier Publishers, 2008

REFERENCE BOOKS:

1. Keating, M., The Simple Art of SoC Design, Springer, 2011.
2. "Embedded System Design: A Unified Hardware/Software Approach" Authors: Frank Vahid and Tony Givargis, Publisher: Wiley

COURSE OUTCOMES:

At the end of the course, students will be able to:

1. Understand and estimate key design metrics and requirements including area, latency, throughput, energy, and power.
2. Implement both hardware and software solutions, formulate hardware/software trade-offs, and perform hardware/software co-design.
3. Analyse issues in system-on-chip design associated with interconnection structures, performance, and power consumption.
4. Use System C programming and high-level synthesis (HLS) for design and modelling.
5. Design and optimize a modern System-on-a-Chip.

II Semester	DETECTION AND ESTIMATION THEORY (D25238B0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce fundamental concepts of random processes including Markov models, point processes, and Gaussian processes.
2. To develop understanding of detection theory using Bayesian and Neyman-Pearson approaches for signal classification under uncertainty.
3. To explore MMSE estimation techniques such as Wiener and Kalman filters for linear and nonlinear systems.
4. To provide knowledge of statistical inference including hypothesis testing, distribution estimation, and regression analysis.
5. To enable parameter estimation of random processes using model-free and model-based approaches with spectral analysis tools.

UNIT –I

Random Processes: Discrete Linear Models, Markov Sequences and Processes, Point Processes, and Gaussian Processes.

UNIT –II

Detection Theory: Basic Detection Problem, Maximum A posteriori Decision Rule, Minimum Probability of Error Classifier, Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal a priori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT –III

Linear Minimum Mean-Square Error Filtering: Linear Minimum Mean Squared Error Estimators; Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT –IV

Statistics: Measurements, Nonparametric Estimators of Probability Distribution and Density Functions, Point Estimators of Parameters, Measures of the Quality of Estimators, Introduction to Interval Estimates, Distribution of Estimators, Tests of Hypotheses, Simple Linear Regression, Multiple Linear Regression.

UNIT –V

Estimating the Parameters of Random Processes from Data: Tests for Stationarity and Ergodicity, Model-free Estimation, Model-based Estimation of Autocorrelation Functions, Power Special Density Functions.

TEXT BOOKS:

1. Steven M. Kay, "Fundamentals of Statistical signal processing, volume 1: Estimation theory". Prentice Hall 2011.
2. Steven M. Kay, "Fundamentals of Statistical signal processing, volume 2: Detection theory". Prentice Hall 2011.

REFERENCE BOOKS:

1. Harry L. Van Trees, "Detection, Estimation, and Modulation Theory, Part I," John Wiley & Sons, Inc. 2011
2. A. Papoulis and S. Unnikrishna Pillai, "Probability, Random Variables and stochastic processes, 4e". The McGraw-Hill 2010

COURSE OUTCOMES:

1. Demonstrate understanding of random processes, including discrete linear models, Markov processes, point processes, and Gaussian processes relevant to signal processing.
2. Apply detection theory to solve problems using MAP, Bayes, and Neyman-Pearson decision rules for both binary and multiple hypothesis testing.
3. Develop and analyze linear and nonlinear minimum mean square error (MMSE) estimators, and design digital Wiener and Kalman filters for signal estimation.
4. Estimate and interpret statistical parameters and distributions using point estimation, nonparametric methods, interval estimates, hypothesis testing, and linear regression models.
5. Evaluate stationarity and ergodicity of random processes and perform both model-free and model-based estimation of autocorrelation and power spectral density functions from data.

II Semester	EMI/ EMC (D25238B1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce enough knowledge regarding the Electromagnetic interference/ Electromagnetic compatibility, Its practical experiences and concerns, and various sources both the natural and nuclear sources of EMI.
2. To know the practical experiences due to EMI such as mains power supply, switches and relays etc and Analyse EM Propagation and Crosstalk
3. To know various methods of the measurements radiated and conducted interference in open area test sites and in chambers.
4. To Learn about the various methods of minimizing the EMI.
5. To know the National/International EMC Standards.

UNIT -I: Introduction, Natural and Nuclear Sources of EMI / EMC:

Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations, An overview of EMI / EMC, Natural and Nuclear sources of EMI.

UNIT -II: EMI from Apparatus, Circuits and Open Area Test Sites:

Electromagnetic emissions, Noise from relays and switches, non-linearities in circuits, passive intermodulation, Cross talk in transmission lines, Transients in power supply lines, Electromagnetic interference (EMI), Open area test sites and measurements.

UNIT -III: Radiated and Conducted Interference Measurements and ESD:

Anechoic chamber, TEM cell, GH TEM Cell, Characterization of conduction currents / voltages, Conducted EM noise on power lines, Conducted EMI from equipment, Immunity to conducted EMI detectors and measurements, ESD, Electrical fast transients / bursts, Electrical surges.

UNIT -IV: Grounding, Shielding, Bonding and EMI filters:

Principles and types of grounding, Shielding and bonding, Characterization of filters, Power lines filter design.

UNIT -V: Cables, Connectors, Components and EMC Standards:

EMI suppression cables, EMC connectors, EMC Gas kets, Isolation Transformers, optoisolators, National / International EMC standards.

TEXT BOOKS:

1. Engineering Electromagnetic Compatibility - Dr. V.P. Kodali, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
2. Electromagnetic Interference and Compatibility IMPACT series, IIT – Delhi, Modules 1-9

REFERENCE BOOKS:

1. Introduction to Electromagnetic Compatibility - Ny, John Wiley, 1992, by C.R. Pal.

COURSE OUTCOMES:

At the end of this course the student can able to:

1. Understand the electromagnetic environment the definitions of EMI and EMC, history of EMI some examples of practical experiences due to EMI such as mains power supply, switches and relays etc.
2. Understand the celestial electromagnetic noise the occurrence of lightning discharge and their effects, the charge accumulation and discharge in an electrostatic discharge, model ESD wave form, the various cases of nuclear explosion and the transients.
3. Understand the methods to measure RE and RS in the open are test sites.
4. Understand the measurement facilities and procedures using anechoic chamber, TEM cell, reverberating chamber GTEM cell.
5. Apply grounding, shielding, bonding techniques, and design EMI filters for interference mitigation.

II Semester	ARM CONTROLLERS AND EMBEDDED C (D25238B2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce ARM processor architecture, instruction sets, and efficient programming techniques.
2. To explore exception handling, memory hierarchy, and management units in ARM systems.
3. To develop embedded system applications using ARM Cortex-M microcontrollers.
4. To implement peripheral interfacing techniques including UART, ADC/DAC, and GPIO.
5. To understand communication protocols like I²C and SPI through practical case studies.

UNIT- I: ARM Processor Fundamentals: ARM Design Philosophy, Registers, CPSR, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions**.**

Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Load Store Instructions, Software Interrupt Instruction, PSR Instructions.

Introduction to the Thumb Instruction Set: Thumb Register Usage, Branch Instructions, Data Processing Instructions, Load-Store Instructions, Stack instructions, Software Interrupt Instruction**.**

Efficient C Programming: Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Structure Arrangement.

Writing and Optimizing ARM Assembly Code: Writing Assembly Code, Profiling and Cycle Counting, Instruction Scheduling, Register Allocation, Conditional Execution, Looping Constructs.

UNIT -II: Exception and Interrupt Handling: Exception Handling, Interrupts, Interrupt Handling Schemes

Caches: The Memory Hierarchy and Cache Memory, Cache Architecture, Cache Policy, Flushing and Cleaning Cache Memory**.**

Memory Protection Units: Protected Regions, Initializing the MPU, Caches and Write Buffer.

Memory Management Units: Moving from an MPU to an MMU, How Virtual Memory Works, Details of the ARM MMU, Page Tables, Translation Lookaside Buffer, Domains And Memory Access Permission, The Fast Context Switch Extension

UNIT- III: Introduction: Definition of Embedded Systems, Real life examples of embedded systems, Basics of Developing for Embedded Systems.

ARM Instruction set Architecture: ARM Cortex-M Organization, Arithmetic, Logical and Shift instructions, Data Movement Instructions, Branch instructions, Program Status register,

Bitwise logic operations, Sign and Zero extension, Data Comparison, Memory addressing, Branch and conditional execution, Control structures, Subroutines, 64-bit data processing.

GPIO: GPIO Input Modes, GPIO Output Modes, Memory-mapped I/O, Push button, Programming exercises on GPIO and Push-button
General-purpose Timers: Clock Configuration, Timer Organization, and Counting Modes, Timer Update Events, PWM Registers, Configuration and initialization of PWM block, Programming exercises on the selection of clock source, Timer's concept, and PWM

UNIT-IV: UART: UART Block, UART Registers, UART baud rate calculation, Configuration and initialization of UART.
ADC/DAC: ADC & DAC registers, pin configuration, ADC modes, Configuring ADC and DAC module, Programming exercises on ADC and DAC
Interfacing: Keypad, LCD, and Seven segment display interfacing with ARM Cortex-M3 Microcontroller

UNIT-V:
Inter-Integrated Circuit (1^2C): I^2C operating modes, Configuration of I^2C, Interface a sensor using I^2C protocol. **Serial Peripheral Interface (SPI):** SPI Modes, Master operation, Slave operation, Configuration of SPI. **Case Study:** Smart Home-Smart Door Locks and Interface a temperature sensor with an I^2C Module to measure the room temperature.

TEXT BOOKS:

1. A.Sloss, D.Symes, C.Wright, "ARM system Developers Guide: Designing and Optimizing System Software", Morgan Kaufmann publishers, 2012.
2. Dr.Yifeng Zhu "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly and C" Third edition, 2018

REFERENCE BOOKS:

1. Steve Furber, "ARM System on Chip Architecture", 2nd ed., Addison Wesley Professional,2000.
2. Valvano, J,"Embedded microcomputer systems: real time interfacing", 3rd Edition, Cengage Learning, 2011.
3. Frank Vahid, TonyGivargis, "Embedded System Design", J Wiley India,2005.
4. Ariel Lutenberg, Pablo Gomez, Eric Pernia "A Beginner's Guide to Designing Embedded System Applications on Arm Cortex-M Microcontrollers"
5. Qing Li, Caroline Yao "Real-time concepts for Embedded Systems" CMP books.

COURSE OUTCOMES:

1. Demonstrate proficiency in ARM instruction sets and assembly code optimization.
2. Configure and manage exceptions, interrupts, and memory systems in ARM-based designs
3. Develop embedded applications using GPIO, timers, and control structures.
4. Interface and program peripherals such as UART, ADC/DAC, and display modules.
5. Apply I²C and SPI protocols in real-world scenarios like smart home systems

II Semester	INTERNET OF THINGS LAB (D2523803)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To introduce students to the fundamentals of IoT architecture and physical layer components.
2. To familiarize students with sensors, actuators, transducers, microcontrollers, and microprocessors used in IoT.
3. To provide hands-on experience with Arduino, Scratch programming, S4A tool, and Arduino IDE.
4. To develop practical skills using Tinker cad simulations and real-time Arduino-based interfaces.
5. To enable interfacing of digital and analog sensors and actuators with Arduino for real-time applications.

List of Experiments:

1. Introduction to IoT, IoT Architecture, introduction to Physical layer
2. Introduction to sensors, actuators, and transducers. Introduction to microcontrollers and microprocessors
3. Introduction to Arduino. Introduction to Scratch programming, S4A tool, and Arduino IDE.
4. Introduction to Tinker cad and some practical examples
5. Working with analog, digital inputs & outputs
6. Interfacing Arduino with Embedded sensors and Actuators
7. Interfacing Arduino with additional sensors
8. Working on Displays and interfacing with Arduino
9. Arduino & LCD Based Projects
10. Arduino interfacing with Keypad and its operation
11. Creating the app (app designing using MIT) and controlling your hardware with your app.
12. Introduction to Node MCU and basic tasks
13. Introduction to Cloud, some IoT Cloud Platforms publishing sensor data to a cloud using Thing speak
14. Controlling your sensor data using Thing speak and MIT APP Inventor
15. Email notifications, app alerts using Blynk cloud
16. Home Automation Using Blynk app

COURSE OUTCOMES:

At the end of the Course the student shall be able to

1. Analyze the concepts of IoT along with its applications.
2. Design a prototype using Arduino Uno.
3. Analyze different types of sensors, actuators and communication Protocols.
4. Execute a prototype of Home Automation using Blynk app.
5. Design an IoT application to interact with cloud.

II Semester	EMBEDDED SYSTEM DESIGN LAB (D2523804)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To introduce students to GPIO configuration and control in embedded systems.
2. To develop skills in serial communication between microcontrollers and PCs using UART.
3. To understand timer and counter functionalities for time delays and interrupts.
4. To provide experience with LCD interfacing and real-time message display.
5. To implement analog-to-digital conversion and PWM signal generation for control applications.

Experiments using ARM Cortex-M Microcontroller: (NUCLEO board -F429ZI):

1. Program to configure and control General Purpose Input / Output (GPIO) port pins.
2. Program to demonstrate Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
3. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment.
4. Program to demonstrate a simple interrupt handler and setting up a timer.
5. Program to Displaying a message in a 2-line x 16 Characters LCD display and verify the result in debug terminal.
6. Program to demonstrate ADC interfacing.
7. Generation of PWM Signal with the objective of introducing the practical application of timers and fundamental principles of control theory.
8. To integrate a micro-SD card with the computing system for the purpose of storing event logs conveniently on the SD card.
9. To establish a connection between the two computing systems using Bluetooth Low Energy (BLE), with the objective of monitoring pertinent information from one system and facilitating gate control through the other system.
10. To enhance the smart home system by enabling it to host a web page through Wi-Fi connectivity, thereby allowing users to access information using a smartphone or PC.

COURSE OUTCOMES:

After successful completion of this lab course, students will be able to:

1. Configure and control GPIO ports and interface with external devices.
2. Implement UART-based serial communication and use debug terminals for testing.
3. Apply timers and counters for generating delays and handling interrupts in real-time systems.
4. Interface LCDs, ADC modules, and generate PWM signals for embedded applications.
5. Store and retrieve event data using SD card integration.

II Semester	SEMINAR – II (D2523804)	L	T	P	C
		0	0	2	1

For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

III Semester	RESEARCH METHODOLOGY AND IPR (D2530000)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamentals of research methodology, including research design and problem formulation.
2. To develop skills for effective literature review, data collection, analysis, and technical writing.
3. To enhance understanding of ethical issues and plagiarism in research.
4. To provide an overview of intellectual property rights, including patents, copyrights, trademarks, and trade secrets.
5. To create awareness about the process of filing IPR and its role in innovation, entrepreneurship, and academic research.

UNIT-I: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II: Effective literature studies approaches, analysis Plagiarism, Research ethics,
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-III: Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV: Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent information and databases, Geographical Indications.

UNIT-V:
New Developments in IPR: Administration of Patent System. New developments in IPR, IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCES:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
3. Mayall, "Industrial Design", McGraw Hill,1992.
4. Niebel, "Product Design", McGraw Hill,1974.
5. Asimov, "Introduction to Design", Prentice Hall,1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New TechnologicalAge",2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008

COURSE OUTCOMES:

At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information and Follow research ethics
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

III Semester	SUMMER INTERNSHIP /INDUSTRIAL TRAINING (D2533801)	L	T	P	C
		0	0	0	3

Students shall undergo mandatory summer internship / industrial training (3 credits) for a minimum of eight weeks duration at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before the committee. The Committee comprises of a HoD / Professor of the department and two faculty. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

III Semester	COMPREHENSIVE VIVA# (D2533802)	L	T	P	C
		0	0	0	2

The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. The examination committee will be constituted by the HoD and Professor of the department and two faculty. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

III Semester	**DISSERTATION PART– A$ (D2533804)**	**L**	**T**	**P**	**C**
		0	**0**	**20**	**10**

IV Semester	**DISSERTATION PART– B% (D2543800)**	**L**	**T**	**P**	**C**
		0	**0**	**32**	**16**

D.N.R. COLLEGE OF ENGINEERING & TECHNOLOGY
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Accredited with A++ Grade by NAAC & Accredited by NBA (B. TECH – CSE, ECE & EEE)
Ph: 08816-221238 Email: dnrcet@gmail.com website: https://dnrcet.org

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

I Year-I Semester M. Tech (Machine Design)	VISION SYSTEMS AND IMAGE PROCESSING (Programme Elective –II)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand basics of machine vision systems and applications.
- Explain image representation and transformation techniques.
- Apply spatial and frequency domain image processing methods.
- Analyse image enhancement and segmentation techniques.
- Evaluate image compression and image analysis methods.

UNIT-I:
Machine vision: Vision sensors - Comparison with other types of sensors- Image acquisition and recognition - Recognition of 3D objects – Lighting techniques - Machine vision applications.

UNIT-II:
Image representation: Application of image processing - Image sampling, Digitization and quantization - Image transforms.

UNIT-III:
Spatial domain techniques: Convolution, Correlation. Frequency domain operations - Fast Fourier transforms, FFT, DFT, Investigation of spectra. Hough transforms.

UNIT-IV:
Image enhancement: Filtering, Restoration, Histogram equalisation, Segmentation, Region growing.

UNIT-V:
Image compression: Edge detection - Thresholding - Spatial smoothing - Boundary and Region representation - Shape features - Scene matching and detection - Image classification.

TEXT BOOKS:

1. Digital Image Processing by Gonzalez, R.C. and Woods, R.E., Addison Wesley Publications.
2 Robot Vision by Prof. Alan Pugh (Editor), IFS Ltd., U.K.
3. Digital Image Processing by A. Rosenfled and A. Kak, Academic Press.

REFERENCES:

1. The Psychology of Computer Vision by P. Winstan, McGraw-Hill.
2. Algorithms for Graphics and Image Processing by T. Pavidis, Springer Verlag.

e-RESOURCES:

- https://nptel.ac.in/courses/117105079.
- https://ocw.mit.edu/courses/6-801-machine-vision-fall-2004.

Annexure-C

Course Code: D2513800

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

MATHEMATICAL FOUNDATION FOR COMMUNICATION ENGINEERING

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain sampling distributions and their importance.	**1**	**2**	**6**
	ii).	Discuss unbiasedness and minimum variance of point estimators with examples.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the steps involved in one-sample hypothesis testing for mean.	**1**	**3**	**6**
	ii).	Compare one-sample and two-sample tests for mean with suitable illustrations.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Define Markov process and explain Markov chain with examples.	**2**	**2**	**6**
	ii).	Explain transition probability matrix and steady-state probabilities.	**2**	**3**	**6**
		OR			
2.B	**i).**	Define a random process and classify random processes.	**2**	**3**	**6**
	ii).	Explain random walk and determine its mean and variance.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Derive Bessel's interpolation formula and state its applicability.	**3**	**3**	**6**
	ii).	Explain Stirling's interpolation formula and compare it with Bessel's formula.	**3**	**4**	**6**
		OR			
3.B	**i).**	Explain the Newton–Raphson method for solving non-linear equations.	**3**	**3**	**6**
	ii).	Describe the fourth-order Runge–Kutta method for solving ODEs.	**3**	**3**	**6**
		UNIT-4			
4.A	**i).**	Explain necessary conditions for optimization of functions of several variables.	**4**	**2**	**6**
	ii).	Discuss sufficient conditions and nature of stationary points.	**4**	**4**	**6**
		OR			
4.B	**i).**	Explain constrained optimization using Lagrange multipliers.	**4**	**3**	**6**

	ii).	Solve an optimization problem using the Lagrange multiplier method.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the concept of multi-resolution analysis.	**5**	**2**	**6**
	ii).	Describe continuous and discrete wavelet transforms.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain the role of wavelet transform in signal analysis.	**5**	**4**	**6**
	ii).	Discuss applications of wavelets in data compression and resolution enhancement.	**5**	**5**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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					Course Code: D2513801
		DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)			**DR25**
		I M. Tech. I Semester MODEL QUESTION PAPER			
		DIGITAL SYSTEM DESIGN			
		For Digital Electronics & Communication Systems			
Time: 3 Hrs.					**Max. Marks: 60 M**
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					5 x 12 = 60 Marks
		UNIT-1	**CO**	**KL**	**M**
1.A	**i).**	Explain Verilog as a Hardware Description Language. Discuss the levels of design description with suitable examples.	**1**	**2**	**6**
	ii).	Describe concurrency in Verilog and explain the difference between simulation and synthesis.	**1**	**3**	**6**
		OR			
1.B	**i).**	Write short notes on modules, system tasks, and parameters in Verilog HDL with examples.	**1**	**4**	**6**
	ii).	Explain the basic language constructs and conventions in Verilog HDL such as identifiers, numbers, logic values, and data types.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain the structure of a Verilog module and describe the AND gate primitive with syntax and example.	**2**	**2**	**6**
	ii).	Design a basic combinational circuit using gate-level modelling and explain its operation.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain tristate gates and array of instances of primitives with suitable examples.	**2**	**3**	**6**
	ii).	Design a D flip-flop using gate primitives and discuss delay and strength resolution.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Explain dataflow modelling in Verilog and describe continuous assignment statements with examples.	**3**	**3**	**6**
	ii).	Design a combinational logic circuit using operators and vector assignments at dataflow level.	**3**	**4**	**6**
		OR			
3.B	**i).**	Explain delays in continuous assignments and parameter usage in dataflow modelling.	**3**	**3**	**6**
	ii).	Write a Verilog program to implement a logic function using dataflow modelling and explain.	**3**	**3**	**6**
		UNIT-4			
4.A	**i).**	Explain the behavioral modelling approach and describe the ‘initial’ construct.	**4**	**2**	**6**

	ii).	Explain functional bifurcation and assignments with delays in behavioral modelling.	**4**	**4**	**6**
		OR			
4.B	**i).**	Explain the 'always' block and wait construct with suitable examples.	**4**	**3**	**6**
	ii).	Design a sequential circuit using multiple always blocks and explain its operation.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Differentiate between blocking and non-blocking assignments with examples.	**5**	**2**	**6**
	ii).	Explain the if–else and case statements used in Verilog procedural blocks.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain looping constructs in Verilog: for, while, repeat, and forever loops.	**5**	**4**	**6**
	ii).	Explain parallel blocks, force–release constructs, and events with suitable examples.	**5**	**5**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D2513801

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

WIRELESS COMMUNICATIONS & NETWORKS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	**CO**	**KL**	**M**
1.A	**i).**	Explain the cellular concept and frequency reuse principle in cellular systems.	**1**	**2**	**6**
	ii).	Explain co-channel interference and adjacent channel interference. Discuss methods to improve system capacity.	**1**	**3**	**6**
		OR			
1.B	**i).**	Discuss channel assignment strategies and power control techniques used for reducing interference.	**1**	**4**	**6**
	ii).	Explain handoff strategies, prioritizing handoffs, and trunking with grade of service.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain the free space propagation model and two-ray ground reflection model.	**2**	**2**	**6**
	ii).	Describe the basic propagation mechanisms: reflection, diffraction, and scattering.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain Okumura and Hata propagation models with their applications.	**2**	**3**	**6**
	ii).	Discuss indoor propagation models and signal penetration into buildings.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Explain small-scale fading and the factors influencing small-scale fading.	**3**	**3**	**6**
	ii).	Explain Doppler spread, coherence time, and coherence bandwidth.	**3**	**4**	**6**
		OR			
3.B	**i).**	Describe the statistical models for multipath fading channels.	**3**	**3**	**6**
	ii).	Explain Rayleigh fading, level crossing rate, and average fade duration.	**3**	**3**	**6**
		UNIT-4			
4.A	**i).**	Explain the fundamentals of equalization in wireless communication systems.	**4**	**2**	**6**
	ii).	Describe LMS and RLS algorithms used for adaptive equalization.	**4**	**4**	**6**
		OR			

4.B	**i).**	Explain linear and non-linear equalizers with suitable block diagrams.	**4**	**3**	**6**
	ii).	Derive selection diversity improvement and maximal ratio combining (MRC).	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain WLAN architecture and IEEE 802.11 MAC protocol.	**5**	**2**	**6**
	ii).	Compare IEEE 802.11 a, b, g, and n standards.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain IEEE 802.16 and its enhancements.	**5**	**4**	**6**
	ii).	Discuss Wireless PANs, HiperLAN, and Wireless Local Loop (WLL).	**5**	**5**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25138A0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

SOFTWARE DEFINED RADIO

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the need and characteristics of Software Defined Radio (SDR).	**1**	**2**	**6**
	ii).	Discuss the benefits and design principles of SDR.	**1**	**2**	**6**
		OR			
1.B	**i).**	Describe traditional hardware radio architecture used in early generation cellular systems.	**1**	**2**	**6**
	ii).	Explain SCR, SDR, ISR, and USR with neat block diagrams.	**1**	**2**	**6**
		UNIT-2			
2.A	**i).**	Explain the purpose of RF front-end in Software Defined Radio.	**2**	**2**	**6**
	ii).	Discuss dynamic range requirements and RF receiver front-end topologies.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain transmitter architectures used in software radio systems.	**2**	**3**	**6**
	ii).	Discuss noise and distortion sources in the RF chain and their impact on performance.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Compare Direct Digital Synthesis with analog signal synthesis.	**3**	**3**	**6**
	ii).	Explain different approaches to Direct Digital Synthesis with block diagrams.	**3**	**3**	**6**
		OR			
3.B	**i).**	Analyse the sources of spurious signals in Direct Digital Synthesis.	**3**	**4**	**6**
	ii).	Explain spurious components due to periodic jitter.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the principles of sample rate conversion.	**4**	**3**	**6**
	ii).	Discuss polyphase filters and their role in multirate signal processing.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain digital filter banks used in multirate systems.	**4**	**3**	**6**

	ii).	Describe timing recovery in digital receivers using multirate digital filters.	**4**	**3**	**6**
		UNIT-5			
5.A	**i).**	Explain ideal parameters of A/D and D/A converters.	**5**	**2**	**6**
	ii).	Discuss practical data converter parameters and techniques to improve performance.	**5**	**3**	**6**
		OR			
5.B	**i).**	Evaluate limitations of practical data converters in SDR systems.	**5**	**4**	**6**
	ii).	Explain the relevance of JTRS and its role in software radio systems.	**5**	**3**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25138A1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

OPTICAL COMMUNICATION & NETWORKS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the elements of an optical fiber transmission link with a neat block diagram.	**1**	**2**	**6**
	ii).	Describe optical fiber structures, fiber types, and modes of propagation.	**1**	**2**	**6**
		OR			
1.B	**i).**	Explain step index and graded index fibers with ray diagrams.	**1**	**2**	**6**
	ii).	Discuss fabrication, cabling, and installation of optical fibers.	**1**	**2**	**6**
		UNIT-2			
2.A	**i).**	Explain the structure and working principle of LEDs used in optical communication.	**2**	**2**	**6**
	ii).	Discuss laser diode threshold condition and modulation capability.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain the working principles of PIN and APD photodiodes	**2**	**3**	**6**
	ii).	Compare optical detectors and discuss noise sources in photodetectors.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Draw and explain the block diagram of an optical communication system.	**3**	**3**	**6**
	ii).	Explain direct intensity modulation and digital optical communication systems	**3**	**3**	**6**
		OR			
3.B	**i).**	Describe the generations of optical fiber communication links.	**3**	**4**	**6**
	ii).	Explain 8 Mb/s and 2.5 Gb/s optical fiber communication links.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain fiber optic network components such as transceivers and optical amplifiers.	**4**	**3**	**6**
	ii).	Describe WDM systems and optical switches used in fiber optic networks.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain SONET/SDH architecture and wavelength routed optical networks.	**4**	**3**	**6**

	ii).	Discuss nonlinear effects and their impact on optical network performance.	**4**	**3**	**6**
		UNIT-5			
5.A	**i).**	Explain coherent optical receivers with homodyne detection.	**5**	**2**	**6**
	ii).	Discuss noise sources and polarization control in coherent receivers.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain heterodyne detection and laser line-width requirements.	**5**	**4**	**6**
	ii).	Describe synchronous, asynchronous, and self-synchronous demodulation techniques.	**5**	**3**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25138A2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

RADIO AND NAVIGATIONAL AIDS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	**i).**	Explain the radio positioning configurations and methods used in terrestrial navigation systems.	**1**	**2**	**6**
	ii).	Discuss the error sources and factors affecting positioning accuracy in radio positioning systems.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the working principle of LORAN with its advantages and limitations.	**1**	**2**	**6**
	ii).	Describe the Instrument Landing System (ILS) and explain its role in aircraft navigation.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Define navigation and explain the concept of position fixing.	**2**	**2**	**6**
	ii).	Explain dead reckoning navigation and its applications in modern navigation systems.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain radio navigation and satellite navigation techniques.	**2**	**2**	**6**
	ii).	Describe the structure and working of a complete navigation system..	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Explain the principle of Differential GNSS (DGNSS) and its accuracy improvement mechanism.	**3**	**3**	**6**
	ii).	Discuss carrier-phase positioning techniques used in satellite navigation.	**3**	**4**	**6**
		OR			
3.B	**i).**	Explain navigation challenges in poor signal-to-noise environments.	**3**	**3**	**6**
	ii).	Analyse multipath effects and describe multipath mitigation techniques.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Derive and explain inertial-frame and Earth-frame navigation equations.	**4**	**3**	**6**
	ii).	Explain local navigation frame equations used in inertial navigation systems.	**4**	**4**	**6**
		OR			

4.B	**i).**	Explain INS initialization and alignment methods.	**4**	**3**	**6**
	ii).	Analyse INS error propagation and its effect on navigation accuracy.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the fundamentals of GNSS systems such as GPS, GLONASS, Galileo, IRNSS.	**5**	**2**	**6**
	ii).	Discuss GNSS measurement errors including ionospheric, tropospheric, and multipath errors.	**5**	**4**	**6**
		OR			
5.B	**i).**	Explain Dilution of Precision (GDOP, PDOP) in satellite navigation.	**5**	**2**	**6**
	ii).	Analyse error correction techniques such as DGNSS, WAAS, and carrier-phase methods.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25138B0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

FPGA and ASIC DESIGN

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the evolution of programmable logic devices and the need for FPGAs.	**1**	**2**	**6**
	ii).	Describe the FPGA design flow and discuss major applications of FPGAs.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the design of a universal logic block using PLDs.	**1**	**3**	**6**
	ii).	Describe the PLD-based design of a barrel shifter or memory block with suitable explanation.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain various FPGA/CPLD programming technologies.	**2**	**2**	**6**
	ii).	Compare SRAM, antifuse, and flash-based programming technologies.	**2**	**3**	**6**
		OR			
2.B	**i).**	Describe the architecture and features of Xilinx Spartan and Virtex FPGAs.	**2**	**3**	**6**
	ii).	Compare Altera and Actel FPGA/CPLD families with suitable examples.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Explain the Configurable Logic Block (CLB) functionality in FPGAs.	**3**	**3**	**6**
	ii).	Describe routing structures and I/O blocks used in FPGA architecture.	**3**	**3**	**6**
		OR			
3.B	**i).**	Analyse the impact of logic block functionality on FPGA performance.	**3**	**4**	**6**
	ii).	Explain the model used for measuring delay in FPGA architectures.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain routing terminology and general routing strategies in FPGAs.	**4**	**3**	**6**
	ii).	Describe routing in row-based FPGAs and segmented channel routing.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain the routing architecture of symmetrical FPGAs with an example.	**4**	**4**	**6**
	ii).	Discuss the general approach to routing in symmetrical FPGAs and independence from routing architectures.	**4**	**4**	**6**
		UNIT-5			

5.A	**i).**	Explain FPGA architectural assumptions and describe the logic block and connection block.	**5**	**3**	**6**
	ii).	Explain the switch block and switch block topology in FPGA architecture.	**5**	**3**	**6**
		OR			
5.B	**i).**	Analyse FPGA architectural features of Kintex-7, Virtex-7, and Artix-7 devices.	**5**	**4**	**6**
	ii).	Discuss real-world applications and case studies implemented using 7-series FPGAs.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25138B1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

SYSTEM DESIGN WITH RTOS AND EMBEDDED LINUX

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the key characteristics of Real-Time Operating Systems (RTOS) and the role of the RTOS kernel and scheduler.	**1**	**2**	**6**
	ii).	Describe task management in RTOS, including task states, scheduling, and task operations.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain RTOS kernel objects, services, and system calls with suitable examples.	**1**	**2**	**6**
	ii).	Discuss task synchronization, communication, and concurrency issues in RTOS-based systems.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain semaphores and their operations. Discuss their use in inter-task synchronization.	**2**	**3**	**6**
	ii).	Describe message queues and other inter-process communication mechanisms such as pipes and signals.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain critical sections and resource synchronization methods in real-time systems.	**2**	**3**	**6**
	ii).	Analyse priority inversion, deadlocks, and common synchronization design problems in RTOS.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Define exceptions and interrupts. Explain their applications in real-time systems.	**3**	**2**	**6**
	ii).	Discuss spurious interrupts and their handling mechanisms in RTOS.	**3**	**4**	**6**
		OR			
3.B	**i).**	Explain timer services in RTOS, including real-time clocks and system clocks..	**3**	**2**	**6**
	ii).	Analyse the role of programmable interval timers and timer interrupt service routines in real-time applications.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the basics of Linux kernel and GNU utilities. Describe different Linux access methods.	**4**	**2**	**6**
	ii).	Describe commonly used Bash shell commands for navigation, file	**4**	**3**	**6**

		handling, and system monitoring.			
		OR			
4.B	**i).**	Explain the steps involved in shell script creation and basic control structures (if-else, loops).	**4**	**3**	**6**
	ii).	Discuss advanced shell scripting features such as signal handling, background scripts, and script functions.	**4**	**3**	**6**
		UNIT-5			
5.A	**i).**	Explain the embedded Linux architecture, including kernel, scheduler, memory manager, and file system.	**5**	**3**	**6**
	ii).	Describe the startup sequence and role of Board Support Package (BSP) in embedded Linux systems.	**5**	**3**	**6**
		OR			
5.B	**i).**	Analyse real-time Linux and hard real-time programming concepts in embedded systems.	**5**	**4**	**6**
	ii).	Explain the process of application porting and driver integration, including bootloader, kernel, root file system, and device tree.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25138B2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

SYSTEM DESIGN USING VERILOG

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain Verilog as a Hardware Description Language and discuss the levels of design description.	**1**	**2**	**6**
	ii).	Explain concurrency in Verilog and describe the simulation and synthesis flow.	**1**	**3**	**6**
		OR			
1.B	**i).**	Describe Verilog language constructs and conventions such as data types, vectors and parameters.	**1**	**2**	**6**
	ii).	Explain operators, logic values and system tasks with suitable examples.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain gate-level modelling and describe basic gate primitives in Verilog.	**2**	**2**	**6**
	ii).	Explain tristate gates, delays and strengths used in gate-level modelling.	**2**	**3**	**6**
		OR			
2.B	**i).**	Design a flip-flop using gate primitives.	**2**	**3**	**6**
	ii).	Explain net types and construction resolution with examples.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain dataflow modelling and the concept of continuous assignment.	**3**	**2**	**6**
	ii).	Explain delays and vector assignments in continuous assignments.	**3**	**3**	**6**
		OR			
3.B	**i).**	Design a combinational circuit using dataflow modelling.	**3**	**3**	**6**
	ii).	Explain the use of parameters and constants in dataflow modelling.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain behavioural modelling and procedural assignments in Verilog.	**4**	**2**	**6**
	ii).	Explain the initial construct and always block with examples.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain assignments with delays and the wait construct.	**4**	**3**	**6**
	ii).	Explain the role of multiple always blocks in behavioural design.	**4**	**4**	**6**
		UNIT-5			

5.A	**i).**	Differentiate between blocking and non-blocking assignments.	**5**	**3**	**6**
	ii).	Explain if–else and case statements in Verilog.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain looping constructs: for, while, repeat and forever.	**5**	**3**	**6**
	ii).	Explain disable, parallel blocks, force–release and event control constructs.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D2523800

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

INFORMATION THEORY AND CODING

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Define information source and entropy. Derive the expression for entropy of a discrete random variable.	**1**	**2**	**6**
	ii).	Explain mutual information and joint & conditional entropy with suitable examples.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain information measures for continuous random variables.	**1**	**2**	**6**
	ii).	Discuss relative entropy and explain any two applications of information theoretic approach.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	State and explain the Source Coding Theorem and Kraft inequality.	**2**	**2**	**6**
	ii).	Explain the construction of Shannon–Fano and Huffman codes.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain Arithmetic coding and Run Length coding with examples.	**2**	**3**	**6**
	ii).	Describe the Lempel–Ziv–Welch (LZW) algorithm and explain the concept of universal source coding.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Define a communication channel and explain channel capacity.	**3**	**2**	**6**
	ii).	Derive the capacity of a discrete memoryless channel (DMC).	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain Gaussian channel and Binary Erasure Channel (BEC).	**3**	**2**	**6**
	ii).	Discuss MIMO channels and explain the effect of feedback on channel capacity.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the basics of video coding and describe quantization and symbol encoding.	**4**	**2**	**6**
	ii).	Explain intraframe coding and interframe coding techniques.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain transform coding and vector quantization used in image compression.	**4**	**3**	**6**

	ii).	Discuss speech coding principles including psycho-acoustic modelling and bit allocation.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Define Hamming weight and minimum distance. Explain error detection and correction theorems.	**5**	**2**	**6**
	ii).	Explain linear block codes, generator matrix and parity check matrix.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain cyclic codes and BCH codes with generator polynomials.	**5**	**3**	**6**
	ii).	Explain convolution codes and the Viterbi decoding algorithm.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D2523801

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

IOT & ITS COMMUNICATION PROTOCOLS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	**i).**	Explain the overall IoT architecture and describe the role of devices and gateways.	**1**	**2**	**6**
	ii).	Explain local and wide area networking in IoT and discuss data management in IoT systems.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain IoT technology fundamentals and the concept of M2M communication.	**1**	**2**	**6**
	ii).	Discuss Everything as a Service (XaaS) and the role of IoT analytics in business processes.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain the IoT reference architecture and describe the functional view.	**2**	**2**	**6**
	ii).	Explain the information view and deployment & operational view of IoT architecture.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain various architectural views used in IoT system design.	**2**	**2**	**6**
	ii).	Discuss real-world technical design constraints encountered in IoT implementations.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain IoT PHY/MAC layer technologies such as IEEE 802.11, IEEE 802.15 and 3GPP MTC.	**3**	**2**	**6**
	ii).	Explain Bluetooth Low Energy, Zigbee and Z-Wave protocols used in IoT.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain IPv6 and 6LoWPAN for IoT networking.	**3**	**2**	**6**
	ii).	Discuss IoT routing protocols such as RPL, CORPL and CARP.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain transport layer protocols TCP and UDP and their relevance to IoT.	**4**	**2**	**6**
	ii).	Explain the role of security protocols TLS and DTLS in IoT communication.	**4**	**3**	**6**
		OR			

4.B	**i).**	Explain session layer protocols HTTP and CoAP for IoT applications.	**4**	**3**	**6**
	ii).	Compare MQTT, AMQP and XMPP with respect to IoT communication requirements.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain IoT service layer protocols such as oneM2M and ETSI M2M.	**5**	**2**	**6**
	ii).	Explain the role of OMA and BBF standards in IoT interoperability.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain security challenges in IoT and the need for protocol-level security.	**5**	**2**	**6**
	ii).	Discuss security mechanisms in IoT protocols at MAC802.15.4, 6LoWPAN, RPL and application layer.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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					Course Code: D2523802
		DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)			**DR25**
		I M. Tech. II Semester MODEL QUESTION PAPER			
		EMBEDDED SYSTEM DESIGN			
		For Digital Electronics & Communication Systems			
Time: 3 Hrs.					**Max. Marks: 60 M**
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					5 x 12 = 60 Marks
		UNIT-1	**CO**	**KL**	**M**
1.A	**i).**	Define an embedded system and compare embedded systems with general-purpose computing systems.	**1**	**2**	**6**
	ii).	Explain the characteristics and quality attributes of embedded systems with suitable examples.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the history and classification of embedded systems.	**1**	**2**	**6**
	ii).	Discuss the major application areas and purpose of embedded systems.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain the core of an embedded system and describe general-purpose and domain-specific processors.	**2**	**2**	**6**
	ii).	Explain ASICs, PLDs and COTS components used in embedded systems.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain memory organization in embedded systems and discuss ROM and RAM types.	**2**	**2**	**6**
	ii).	Discuss sensors, actuators and communication interfaces (onboard and external) used in embedded systems.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain the need and operation of reset circuit and brown-out protection circuit in embedded systems.	**3**	**2**	**6**
	ii).	Explain the functions of oscillator unit, real-time clock and watchdog timer.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain the embedded firmware architecture and its key building blocks.	**3**	**2**	**6**
	ii).	Discuss embedded firmware design approaches and development languages.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the ARM design philosophy and describe the ARM core architecture and registers.	**4**	**2**	**6**
	ii).	Explain the program status register (PSR) and instruction pipeline in ARM processors.	**4**	**3**	**6**

		OR			
4.B	**i).**	Explain ARM interrupts, vector table and operating modes.	**4**	**2**	**6**
	ii).	Explain ARM instruction sets: data processing, addressing modes, load/store and conditional instructions.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the Raspberry Pi board architecture and its processor features.	**5**	**2**	**6**
	ii).	Explain programming the Raspberry Pi using Python.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain the communication interfaces of Raspberry Pi: I2C, SPI and UART.	**5**	**3**	**6**
	ii).	Discuss interfacing of sensors and actuators with Raspberry Pi for embedded applications.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25238A0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

DESIGN FOR TESTABILITY

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the testing philosophy and the role of testing in VLSI systems.	**1**	**2**	**6**
	ii).	Explain fault modelling in digital circuits and describe the single stuck-at fault model.	**1**	**3**	**6**
		OR			
1.B	**i).**	Differentiate between functional testing and structural testing.	**1**	**2**	**6**
	ii).	Discuss VLSI technology trends affecting testing and types of testing.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain the need for simulation in design verification and test evaluation.	**2**	**2**	**6**
	ii).	Describe the true-value simulation algorithm with suitable examples.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain modelling of circuits for simulation in VLSI testing.	**2**	**2**	**6**
	ii).	Explain fault simulation algorithms used for test evaluation.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain SCOAP controllability and observability measures.	**3**	**2**	**6**
	ii).	Explain high-level testability measures used in digital circuits.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain ad-hoc DFT methods used to improve testability.	**3**	**2**	**6**
	ii).	Explain scan design and partial-scan design techniques.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the economic motivation for BIST and describe the BIST process.	**4**	**2**	**6**
	ii).	Explain pattern generation and response compaction in logic BIST.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain random logic BIST and test-per-clock BIST systems.	**4**	**3**	**6**
	ii).	Explain memory BIST and delay fault BIST techniques.	**4**	**4**	**6**

		UNIT-5			
5.A	**i).**	Explain the motivation for boundary scan and describe the TAP controller and TAP port.	**5**	**2**	**6**
	ii).	Explain boundary scan test instructions and pin constraints of the standard.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain the boundary scan architecture used in board-level testing.	**5**	**2**	**6**
	ii).	Explain Boundary Scan Description Language (BSDL) and its description components.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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					Course Code: D25238A1
		DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)			**DR25**
		I M. Tech. II Semester MODEL QUESTION PAPER			
		MEMS			
		For Digital Electronics & Communication Systems			
Time: 3 Hrs.					**Max. Marks: 60 M**
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					5 x 12 = 60 Marks
		UNIT-1	**CO**	**KL**	**M**
1.A	**i).**	Differentiate between microsystems and MEMS. Explain the concept of integrated microsystems.	**1**	**2**	**6**
	ii).	Explain smart materials and discuss their applications in MEMS and microsystems.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the basic concepts of microfabrication in MEMS.	**1**	**2**	**6**
	ii).	Discuss the structures and systems in MEMS and their application areas.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain the working principle of a silicon capacitive accelerometer.	**2**	**2**	**6**
	ii).	Explain the operation of a piezoresistive pressure sensor with neat diagrams.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain the working of an electrostatic comb-drive actuator.	**2**	**2**	**6**
	ii).	Discuss any two MEMS-based smart systems such as micro-mirror array, inkjet print head, or portable blood analyzer.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain silicon as a material for micromachining and its advantages.	**3**	**2**	**6**
	ii).	Explain thin-film deposition techniques used in MEMS fabrication.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain lithography and etching processes used in microfabrication.	**3**	**2**	**6**
	ii).	Discuss advanced microfabrication processes and specialized materials for microsystems.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the mechanical modelling of a bar as a deformable element in MEMS.	**4**	**2**	**6**
	ii).	Explain the bending behaviour of beams using energy methods.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain heterogeneous layered beams and the bimorph effect	**4**	**3**	**6**

	ii).	Discuss residual stresses, Poisson effect, and anticlastic curvature in MEMS beams.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the need for numerical methods and the basic concept of Finite Element Method (FEM).	**5**	**2**	**6**
	ii).	Explain the steps involved in FEM modelling of MEMS structures.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain the finite element model for structures with piezoelectric sensors and actuators**.**	**5**	**2**	**6**
	ii).	Discuss the FEM analysis of a piezoelectric bimorph cantilever beam**.**	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25238A2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

SYSTEM ON CHIP DESIGN

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	**i).**	Explain the basic concepts of chips and System-on-Chip (SoC) ICs.	**1**	**2**	**6**
	ii).	Describe the major components of an SoC such as CPU/IP cores, coprocessors, cache and DRAM controller.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the SoC design flow including synthesis, static timing analysis, verification and physical design.	**1**	**2**	**6**
	ii).	Discuss the role of design for testability (DFT) in SoC implementation.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain hardware–software partitioning in SoC design.	**2**	**2**	**6**
	ii).	Discuss area, time, power and cost trade-offs in hardware–software co-design.	**2**	**2**	**6**
		OR			
2.B	**i).**	Explain real-time scheduling issues in SoC-based systems.	**2**	**3**	**6**
	ii).	Explain the concept of hardware acceleration and its impact on system performance.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain virtual prototyping and its importance in system-level design.	**3**	**2**	**6**
	ii).	Explain transaction-level modeling (TLM) and electronic system-level (ESL) languages.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain the process of mapping high-level language applications to hardware.	**3**	**3**	**6**
	ii).	Discuss high-level synthesis (C-to-RTL) and source-level optimizations.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain bus-based interconnection structures in SoCs.	**4**	**2**	**6**
	ii).	Explain the features of AMBA AXI and AXI4-Stream protocols.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain Network-on-Chip (NoC) architecture and its advantages over buses.	**4**	**2**	**6**

	ii).	Discuss IP interfacing issues in NoC-based SoC systems.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain system-level modeling and integration in SoC design.	**5**	**2**	**6**
	ii).	Explain simulation platforms used for performance analysis of SoC/MPSoC.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain performance and power metrics used in SoC evaluation.	**5**	**3**	**6**
	ii).	Discuss use cases and examples for system-level performance and power analysis.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25238B0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

DETECTION AND ESTIMATION THEORY

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	**i).**	Explain discrete linear models and their significance in modelling random processes.	**1**	**2**	**6**
	ii).	Discuss Markov sequences and Markov processes with suitable examples.	**1**	**3**	**6**
		OR			
1.B	**i).**	Describe point processes and their applications in signal processing.	**1**	**2**	**6**
	ii).	Explain the characteristics and properties of Gaussian random processes**.**	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain the basic detection problem and derive the MAP decision rule.	**2**	**3**	**6**
	ii).	Describe the minimum probability of error classifier using Bayes decision theory.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain the Neyman–Pearson criterion for binary hypothesis testing.	**2**	**3**	**6**
	ii).	Discuss the general Gaussian detection problem and computation of probability of error.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Derive the linear minimum mean square error (LMMSE) estimator.	**3**	**3**	**6**
	ii).	Explain nonlinear MMSE estimation and the concept of innovations.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain the design and operation of digital Wiener filters with stored data.	**3**	**3**	**6**
	ii).	Describe the Kalman filter algorithm and its applications.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain nonparametric estimators of probability density functions.	**4**	**2**	**6**
	ii).	Discuss point estimators and measures of the quality of estimators.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain the concepts of interval estimation and distribution of estimators.	**4**	**3**	**6**
	ii).	Describe tests of hypotheses and explain simple linear regression.	**4**	**4**	**6**

		UNIT-5			
5.A	**i).**	Explain tests for stationarity and ergodicity of random processes.	**5**	**3**	**6**
	ii).	Discuss model-free estimation of random process parameters.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain model-based estimation of autocorrelation functions.	**5**	**3**	**6**
	ii).	Describe methods for estimating power spectral density functions from data.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25238B1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

EMI/ EMC

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the electromagnetic environment and basic concepts of EMI and EMC.	**1**	**2**	**6**
	ii).	Discuss the history, practical experiences, and concerns related to EMI in engineering systems.	**1**	**3**	**6**
		OR			
1.B	**i).**	Describe the frequency spectrum conservation and its importance in EMC.	**1**	**2**	**6**
	ii).	Explain the natural and nuclear sources of EMI and their effects on electronic systems.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain electromagnetic emissions due to relays, switches, and non-linear circuit elements.	**2**	**3**	**6**
	ii).	Discuss passive intermodulation and crosstalk in transmission lines.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain transients in power supply lines and their role in EMI generation.	**2**	**3**	**6**
	ii).	Describe open area test sites (OATS) and methods used for EMI measurements.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain the construction and working of an anechoic chamber and TEM cell.	**3**	**2**	**6**
	ii).	Discuss characterization of conducted currents and voltages on power lines.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain conducted EMI from equipment and methods of immunity measurement.	**3**	**3**	**6**
	ii).	Describe Electrostatic Discharge (ESD), EFT/bursts, and electrical surge phenomena.	**3**	**3**	**6**
		UNIT-4			
4.A	**i).**	Explain the principles and types of grounding used in EMC applications.	**4**	**2**	**6**
	ii).	Discuss shielding and bonding techniques for EMI control.	**4**	**3**	**6**

		OR			
4.B	**i).**	Explain the characterization of EMI filters.	**4**	**3**	**6**
	ii).	Describe the design of power line filters for EMI suppression.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain EMI suppression cables and EMC connectors.	**5**	**2**	**6**
	ii).	Discuss the role of EMC gaskets, isolation transformers, and opto-isolators.	**5**	**3**	**6**
		OR			
5.B	**i).**	Describe the need and importance of EMC standards.	**5**	**2**	**6**
	ii).	Explain national and international EMC standards with examples.	**5**	**3**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Course Code: D25238B2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

ARM CONTROLLERS AND EMBEDDED C

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the ARM design philosophy, register organization, and CPSR with suitable diagrams.	**1**	**2**	**6**
	ii).	Discuss the ARM instruction set covering data processing, load–store, branch, and PSR instructions.	**1**	**3**	**6**
		OR			
1.B	**i).**	Describe the Thumb instruction set, register usage, and advantages over ARM instructions.	**1**	**2**	**6**
	ii).	Explain efficient C programming techniques and ARM assembly code optimization methods.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain exception and interrupt handling mechanisms in ARM processors with vector table.	**2**	**3**	**6**
	ii).	Discuss the ARM memory hierarchy and cache architecture, including cache policies.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain the Memory Protection Unit (MPU) and its initialization in ARM systems.	**2**	**3**	**6**
	ii).	Describe the ARM Memory Management Unit (MMU), virtual memory concept, and TLB.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain the ARM Cortex-M architecture and instruction categories with examples.	**3**	**2**	**6**
	ii).	Discuss branching, conditional execution, and subroutines in ARM Cortex-M.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain GPIO input/output modes and memory-mapped I/O with push-button interfacing.	**3**	**4**	**6**
	ii).	Describe the working and configuration of general-purpose timers and PWM generation.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the UART block, registers, and baud rate calculation in ARM Cortex-M.	**4**	**3**	**6**

	ii).	Describe UART initialization and data transmission/reception with suitable flow.	**4**	**4**	**6**
		OR			
4.B	**i).**	Explain ADC architecture, modes of operation, and configuration in ARM microcontrollers.	**4**	**3**	**6**
	ii).	Discuss interfacing of LCD / keypad / seven-segment display with ARM Cortex-M.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the I^2C protocol, operating modes, and configuration steps in ARM controllers.	**5**	**3**	**6**
	ii).	Describe sensor interfacing using I^2C with a suitable example.	**5**	**4**	**6**
		OR			
5.B	**i).**	Explain the SPI protocol, modes of operation, and master–slave communication.	**5**	**3**	**6**
	ii).	Discuss the Smart Home – Smart Door Lock case study using ARM Cortex-M.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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					Course Code: D2530000
		DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)			**DR25**
		II M. Tech. III Semester MODEL QUESTION PAPER			
		RESEARCH METHODOLOGY AND IPR			
		For Digital Electronics & Communication Systems			
Time: 3 Hrs.					**Max. Marks: 60 M**
		Answer **ONE Question** from **EACH UNIT**			
		Assume suitable data if necessary			
					5 x 12 = 60 Marks
		UNIT-1	**CO**	**KL**	**M**
1.A	**i).**	Discuss use cases and examples for system-level performance and power analysis.	**1**	**2**	**6**
	ii).	Elaborate on common errors committed by researchers in selecting the research problem.	**1**	**3**	**6**
		OR			
1.B	**i).**	Give a detailed account on various approaches adopted by researchers in solving problems stated by them.	**1**	**2**	**6**
	ii).	Explain with neat sketches, various charts used in presentation of data.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	What are the different ethical issues related to authorship?	**2**	**2**	**6**
	ii).	List and explain the guidelines for Effective technical writing.	**2**	**3**	**6**
		OR			
2.B	**i).**	List and elaborate the different sources of literature studies.	**2**	**2**	**6**
	ii).	How will you prepare the timeframe, activity schedule, budget plan for your proposed research?	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	List the different considerations in choosing a particular research contribution for patenting.	**3**	**2**	**6**
	ii).	What is IPR? Give examples.	**3**	**3**	**6**
		OR			
3.B	**i).**	Elaborate the concepts of creativity and innovation.	**3**	**2**	**6**
	ii).	Explain how patents are filed under PCT.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	What is the transfer of technology in patent rights? Explain	**4**	**2**	**6**
	ii).	How patent information's are protected? Discuss.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain Geographical Indications.	**4**	**3**	**6**

	ii).	What is the information that can be gathered from patent database? Discuss.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the Emerging issues in IPR.	**5**	**2**	**6**
	ii).	Describe the administration of Patent system.	**5**	**3**	**6**
		OR			
5.B		Discuss in detail about IPR of Biological Systems.	**5**	**2**	**12**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks