ECE Department

3rd BOS File

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

CIRCULAR

This is to inform all ECE Department BoS members that the 3rd Board of Studies (BoS) meeting will be held on Friday, January 9, 2026, at 10:00 AM via online mode (Zoom) from the MPMC Lab. You are all cordially invited to attend; the meeting link will be shared via email.

Agenda

1. **Welcome Speech by the Chairperson.**
2. **Introducing the members of the Board of Studies.**
3. **To discuss and finalize the proposed III B. Tech. I & II Semester Course structure and Syllabus of DR24 Regulations.**
4. **To discuss and finalize the proposed M. Tech. Course structure and Syllabus of DR25 Regulations.**
5. **Ratification of Course Objectives and Course Outcomes for the proposed Curriculum.**
6. **Finalization of Model Question Papers and List of Paper Setters.**
7. **Any other item with the permission of the chair**

Head of the Department & BoS Chairman

Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Copy To:

1. **The Members of the BoS**
2. **The Principal**
3. **The Dean (Academics)**
4. **To the Office File**

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

Dr. B. T Krishna,
Professor, ECE Department,
University College of Engineering,
Kakinada, AP-533003.

Dear sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

We take the privilege in inviting you for the Board of Studies (BoS) 3rd meeting of the ECE department, DNR College of Engineering & Technology(9P) as a Subject Expert from outside the parent university. It is proposed to discuss and finalize the following for the A.Y. 2026- 27.

1. Welcome Speech by the Chairperson.
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Kindly accept our invitation and make it convenient to attend the Board of Studies meeting.

Yours Sincerely,

K Venu Gopal

(Dr. K. Venu Gopal)

HoD and Chairman BoS.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

To

Dr. N. Udaya Kumar,
Professor, ECE Department,
SRKR Engg. College (Autonomous),
Bhimavaram, AP-534202.

Dear Sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

To

Dr. P. Srinivasa Rao,
Assoc. Professor, ECE Department,
St. Anna's College of Engineering & Technology (Autonomous),
Chirala, AP – 523187.

Dear sir,

Sub: DNR College of Engineering & Technology, ECE Dept-Board of Studies Meeting-Reg.

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(Dr. K. Venu Gopal),

HoD and Chairman BoS.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

Mrs. I. Pavani,
2016-20 Batch,
Roll No.169P1A0416,
Bhimavaram,
AP-534202.

Dear sir,

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
Dt: 07/01/2026.

Mr. Sriramulu Govada,
Design. Technical Officer 'A',
DRDO, Visakhapatnam,
AP-530027.

Dear sir,

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Yours Sincerely,

(Dr. K. Venu Gopal)

HoD and Chairman BoS.

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

1 message

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 12:59 PM
To: tkbattula@jntucek.ac.in

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

--
With Warm regards
HOD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Dr.B.T Krishna.pdf
364K

Gmail ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

2 messages

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 12:58 PM
To: Uday N <udayvas2005@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

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With Warm regards
HOD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Dr.N.Uday Kumar.pdf
345K

Uday N <udayvas2005@gmail.com> Thu, Jan 8, 2026 at 4:23 PM
To: ELECTRONICS <dnrcetece@gmail.com>

Ok sir.
All the best sir

with best wishes and regards
Dr. N. Udaya Kumar M. Tech, Ph. D, MISTE, MSIOI,MBMESI,MSEMCE(I),FIE,FIETE
Senior Member IEEE(SMIEEE),
Professor and Head, Department of ECE,
SRKR Engineering College,
Bhimavaram
Ex-Secretary, IEEE Comsoc/SP Societies Joint Chapter, IEEE Vizag Bay Section
Ex-AP State Committee Member (IE)- ET Division
Mobile: 9440354093(Whatsapp)
:6300465439(Whatsapp)
[Quoted text hidden]

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

1 message

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 12:55 PM
To: Srinivas Rao <psraoece@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

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With Warm regards
HoD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Dr.P.Srinivasa Rao.pdf
374K

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

1 message

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 1:01 PM
To: Sriram Govada <sriramgovada@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

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With Warm regards
HOD
Dept. of ECE
DNRCET
Bhimavaram, W.G.Dist.,
A.P-534202.

Mr.Sriamulu Govada.pdf
352K

Gmail

ECE DEPARTMENT ECE <dnrcetece@gmail.com>

Invitation to the 3rd Board of Studies (BoS) Meeting – ECE Department, DNRCET

ELECTRONICS <dnrcetece@gmail.com> Thu, Jan 8, 2026 at 1:01 PM
To: Pavani Indukuri <pavaniindukuri123@gmail.com>

Respected sir ,

Greetings from the Department of Electronics and Communication Engineering, DNR College of Engineering and Technology!

On behalf of the ECE Department, we are pleased to cordially invite you to attend the 3rd Board of Studies (BoS) Meeting of our department. Your valuable presence and insights will greatly contribute to our academic discussions and curriculum development.

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With Warm regards
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I.Pavani.pdf
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Bhimavaram,
09/01/2026.

Ref: DNRCET/ECED/2025-26/BOS-MOM/1

Minutes of Meeting (MOM) of the Board of Studies (BOS)

The 3rd Board of Studies (BoS) meeting for the Electronics & Communication Engineering (ECE) Department took place on Friday, January 9, 2026, via Zoom in the MPMC Lab. The session focused on reviewing the proposed agenda and adopting key resolutions.

Meeting link

https://us06web.zoom.us/j/88650471236?pwd=sozL2jB9kdnblbXv6n0XF4t6oGuzel.

Agenda:

1. **Welcome Speech by the Chairperson.**
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3. **To discuss and finalize the proposed III B. Tech. I & II Semester Course structure and Syllabus of DR24 Regulations.**
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6. **Finalization of Model Question Papers and List of Paper Setters.**
7. **Any other item with the permission of the chair**

The following members attended the meeting:

Name(s) of the Member(s)/Nominee(s)	Designation in Committee	Signature
Dr. K. Venu Gopal	**Chairperson**	K Venu Gopal
Dr. B. T Krishna, Professor, ECE Department, University College of Engineering, Kakinada, AP-533003. e-mail: tkbattula@jntucek.ac.in Mobile: 9502770755.	**Member** **(University Nominee)**	Attended ONLINE

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Dr. N. Udaya Kumar, Professor, ECE Dept, SRKR Engineering. College (Autonomous), Bhimavaram-534202, e-mail: nuk@srkrec.ac.in Mobile: 9440354093.	**Member** **(Subject experts from outside the parent University)**	Attended ONLINE
Dr. P. Srinivasa Rao, Assoc. Professor, ECE Dept., St. Anna's College of Engineering & Technology (Autonomous), Chirala-523187 e-mail: psraoece@gmail.com Mobile: 6281266754.	**Member** **(Subject experts from outside the parent University)**	Attended ONLINE
Mr. Sriramulu Govada, Design. Technical Officer 'A', DRDO, Visakhapatnam, e-mail: sriramgovada@gmail.com Mobile: 9492126360.	**Member** **(Industrial Expert)**	Attended ONLINE
Mrs. I. Pavani, 2016-20 Batch, Roll No.169P1A0416, e-mail: pavaniindukuri123@gmail.com, Mobile No: 63039 84842.	**Member** **(College alumni)**	Attended ONLINE
Dr. Nekkanti Venkata Rao	**Members** **of the Department**	
Dr A. Purna Ramesh		
Dr. S. Ravi chandh		
Mr. Kopalli Venkanna Naidu		
Mr. Kurma Sekhar Babu		
Mrs.N.S.V.L. Sowjanya		

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Mr. K. Satish Kumar		
Mrs. N Mary Leena		
Mr.M. Venu		
Mr. S. Apparao		
Mrs.K Indira Priyadarsini		
Mrs. B. Nagamani		
Mr. P. Gopala Swami		
Mrs. K. Krishna Deepika		
Mrs. P. Srivalli		
Mr. Vendra Bhavani Durga		
Mrs. K. Durga		
Mrs. U. Sai Mounica		
Mr.S. Joseph		
Mrs.P. Pardhavi		
Mr. P Narasimha Murthy		
Mr.V. Phani Kiran		
Ms.N. Sowjanya		N. Sowjanya
Ms.K. Uma devi		K. Umadevi
Mr.G. Manikanta		G. Manikanta
Mr.T Srinivas		
Mr.J.S.S. Ramaraju		
Ms. S.R..S. Anusha		
Ms.G. Chinnari		G. Chinnari

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

The Principal of DNRCET opened the meeting by thanking the university nominee and all BoS members. Dr. K. Venu Gopal, Chairman of the ECE BoS, then took charge of the proceedings. The meeting concluded with the following key resolutions:

Resolutions:

Agenda Point 1: Welcome speech by the chairperson

Resolution: Dr. K. Venu Gopal, Chairman of the BoS, warmly welcomed all BoS members.

Agenda Point 2: Introduction of members

Resolution: The Chairman of BoS, Dr. K. Venu Gopal, welcomed all the members and introduced internal BoS members to external BoS members.

The meeting began with the III B. Tech curriculum presentation for semesters I & II.

Agenda Point 3: To discuss and finalize the proposed III B. Tech-I & II Semester ECE (Theory and Lab) courses of DR24 Regulations.

Resolution: After clearly discussing every unit of theory courses curses

III B. Tech-I Semester DR24 Syllabus (Theory & Labs)- including professional Electives curses 1. Analog & Digital IC Applications, 2. Digital communications, 3. Antennas and Wave Propagation,4. Digital System Design through HDL, 5. Optical Communications, 6. Electronic Measurements and Instrumentation, 7. Computer Organization and Architecture, 8. Analog & Digital IC Applications Lab, 9. Analog and digital communications Lab. 10. Applications of Lab view for Instrumentation & Communications, 11. Design of PCB & Antennas Lab.

III B. Tech-II Semester DR24 Syllabus (Theory & Labs)- including professional Electives curses 1. VLSI Design, 2. Microprocessors & Microcontrollers, 3. Digital Signal Processing, 4. Analog IC Design, 5. Satellite Communication, 6. Smart and Wireless Instrumentation, 7. Machine Learning, 8. Bio Medical Instrumentation, 9. Microwave Engineering, 10. Embedded Systems, 11. Artificial Intelligence, 12. VLSI Design Lab, 13. Microprocessors & Microcontrollers Lab, 14. Machine Learning Lab

List of Open Elective courses offered by department of ECE:

Pool 1: Open Elective 1 (Either of the 4 subjects)-

1. Electronic Devices and Circuits, 2. Signals and Systems, 3. Probability Theory and Random Variables, 4. Network Analysis

Pool 2: Open Elective 2 (Either of the 4 subjects)-

1. Linear and Digital IC Applications, 2. Principles of Communications, 3. Principles of Signal Processing, 4. Microprocessors & Microcontrollers.

Pool 3: Open Elective 3 (Either of the 4 subjects)-

1. Fundamentals of VLSI Design, 2. Digital Electronics, 3. Electronic Measurements and Instrumentations, 4. Optical Communications.

Pool 4: Open Elective 4 (Either of the 4 subjects)-

1. Principles of Cellular & Mobile Communications, 2. Fundamentals of Satellite Communications, 3. Embedded Systems, 4. Transducers and Signal Conditioning.

Annexure-A **(Enclosed Annexure-A).**

Agenda Point 4: To discuss and finalize the proposed M. Tech. Course structure and Syllabus of DR25 Regulations.

Resolution: After clearly discussing every unit of theory courses,

M. Tech DR25 I Semester Syllabus (Theory & labs)-1. including professional Electives curses 1.Mathematical Foundation for Communication Engineering, 2. Digital System Design, 3. Wireless Communications & Networks, 4. Software Defined Radio, 5. Optical Communication & Networks, 6. Radio and Navigational Aids, 7. FPGA and ASIC Design, 8. System Design with RTOS & Embedded LINUX, 9. System Design Using Verilog, 10. Digital System Design Laboratory, 11. Wireless Communications Laboratory, 12. Seminar.

M. Tech DR25 II Semester Syllabus (Theory & labs)-1. including professional Electives curses 1.Information Theory and Coding, 2. IoT & its Communication Protocols, 3. Embedded System Design, 4. Design for Testability, 5. MEMS, 6. System on Chip Design, 7. Detection and Estimation Theory, 8. EMI/ EMC, 9. ARM Controllers and Embedded C, 10. Internet of Things Lab, 11. Embedded System Design Lab, 12. Seminar.

M. Tech DR25 III & IV Semester Syllabus (Theory & labs)-1. Research Methodology and IPR/Swayam 12-week MOOC course – RM & IPR, 2. Summer Internship / Industrial Training, 3. Comprehensive Viva, 8. Project Work (Dissertation Part – A).

IV Semester Syllabus (Theory & labs)

1,Project Work (Dissertation Part – B)

Other Branches Subjects: 1. Vision Systems and Image Processing.

II. Annexure-B **(Enclosed Annexure -B).**

Agenda Point- 5: Ratification of Course Objectives and Course Outcomes for the proposed subjects.

Resolution: Following detailed discussions, the BoS approved the proposed Course Objectives and Outcomes, incorporating the modifications made to the theory courses and labs outlined in agenda items 3 and 4.

Agenda Point- 6: Finalization of Model Paper. `

Resolution: The BoS members recommended aligning Course Outcomes (COs) with the sequence of exam questions, replacing Knowledge Level (KL) with Bloom's Taxonomy Level (BL), and assigning 4 or 6 marks to select long-answer questions (out of 10). Following confirmation of the COs, BL levels, and marking scheme, the BoS approved the proposed model question papers for external theory course examinations. Annexure-C **(Enclosed Annexure -C).**

Agenda Point 7: Any other item with the permission of the chair.

Resolution: The Chairman of the Board of Studies emphasized the importance of MOOCs and SWAYAM/NPTEL courses for enhancing student skills. He also outlined honors and minor courses, aligned with APSCHE and JNTUK Kakinada guidelines

In conclusion, the Chairman summarized the agenda and resolutions, extended a vote of thanks, and appreciated every member's cooperative effort

Note: All conversations from the BoS meetings are captured on the Zoom platform and kept in the Department's records.

Chairman, BoS

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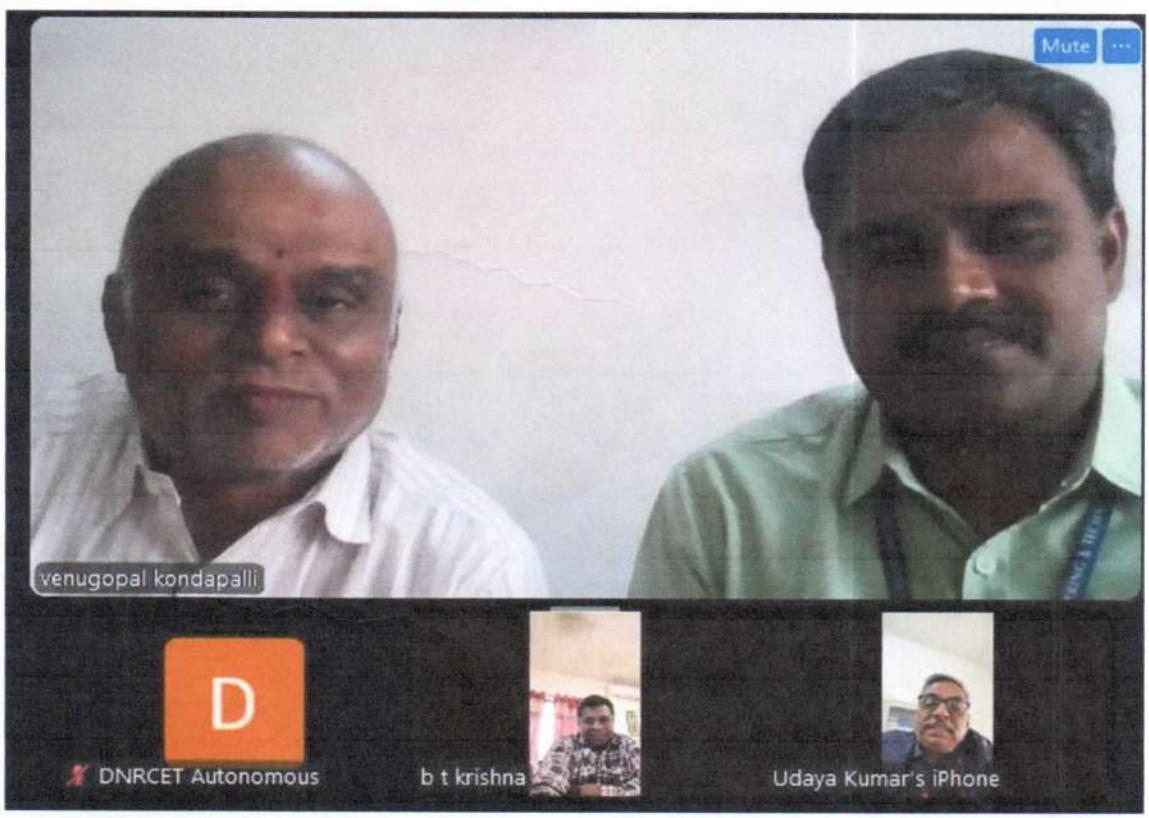
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Bhimavaram,
09/01/2026.

Ref: DNRCET/ECED/2026-27/BOS-photos/1



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Chairman, BoS

Annexure-A

DR24

B.Tech

Course Structure

&

Syllabus

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech. III Year I Semester

S.No.	Category	Title	Course Code	L	T	P	C
1	PC	Analog & Digital IC Applications	BT24EC3101	3	0	0	3
2	PC	Digital communications	BT24EC3102	3	0	0	3
3	PC	Antennas and Wave Propagation	BT24EC3103	3	0	0	3
4	PE-I	1. Digital System Design through HDL 2. Optical Communications 3. Electronic Measurements and Instrumentation 4. Computer Organization and Architecture	BT24EC31P1A BT24EC31P1B BT24EC31P1C BT24EC31P1D	3	0	0	3
5	OE-I	OR Entrepreneurship Development & Venture Creation	BT24HS3101	3	0	0	3
6	PC	Analog & Digital IC Applications Lab	BT24EC3104	0	0	3	1.5
7	PC	Analog and digital communications Lab	BT24EC3105	0	0	3	1.5
8	SEC	Applications of Lab view for Instrumentation & Communications	BT24EC3106	0	1	2	2
9	ES	Design of PCB & Antennas Lab	BT24EC3107	0	0	2	1
10	Evaluation of Community Service Internship		BT24BS3103	-	-	-	2
Total				**15**	**1**	**10**	**23**
MC	Minor Course (Student may select from the same specialized minors pool)			3	0	3	4.5
MC	Minor Course through SWAYAM / NPTEL (Minimum 12 Week, 3 credit course)			3	0	0	3
HC	Honors Course (Student may select from the same Honors pool)			3	0	0	3
HC	Honors Course (Student may select from the same Honors Pool)			3	0	0	3

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B.Tech. III Year II Semester

S.No.	Category	Title	Course Code	L	T	P	C
1	PC	VLSI Design	BT24EC3201	3	0	0	3
2	PC	Microprocessors & Microcontrollers	BT24EC3202	3	0	0	3
3	PC	Digital Signal Processing	BT24EC3203	3	0	0	3
4	PE-II	1. Analog IC Design 2. Satellite Communication 3. Smart and Wireless Instrumentation 4. Machine Learning	BT24EC32P2A BT24EC32P2B BT24EC32P2C BT24EC32P2D	3	0	0	3
5	PE-III	1. Bio Medical Instrumentation 2. Microwave Engineering 3. Embedded Systems 4. Artificial Intelligence	BT24EC32P3A BT24EC32P3B BT24EC32P3C BT24EC32P3D	3	0	0	3
6	OE-II	Open Elective from Another Department		3	0	0	3
7	PC	VLSI Design Lab	BT24EC3204	0	0	3	1.5
8	PC	Microprocessors & Microcontrollers Lab	BT24EC3205	0	0	3	1.5
9	SEC	Machine Learning Lab	BT24EC3206	0	1	2	2
10	AC	Research Methodology and IPR	BT24HS3201	2	0	0	-
Total				**20**	**1**	**08**	**23**
Mandatory Industry Internship of 08 weeks duration during summer vacation							
MC	Student may select from the same minor's pool			3	0	3	4.5
MC	Minor Course (Student may select from the same specialized minors pool)			3	0	0	3
HC	Student may select from the same honors pool			3	0	0	3
HC	Honors Course (Student may select from the honors pool)			3	0	0	3

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List of Open Elective courses offered by department of ECE:

Pool 1: Open Elective 1 (Either of the 4 subjects)

1. Electronic Devices and Circuits - BT24EC31O1A
2. Signals and Systems - BT24EC31O1B
3. Probability Theory and Random Variables - BT24EC31O1C
4. Network Analysis - BT24EC31O1D

Pool 2: Open Elective 2 (Either of the 4 subjects)

1. Linear and Digital IC Applications - BT24EC32O2A
2. Principles of Communications - BT24EC32O2B
3. Principles of Signal Processing - BT24EC32O2C
4. Microprocessors & Microcontrollers - BT24EC32O2D

Pool 3: Open Elective 3 (Either of the 4 subjects)

1. Fundamentals of VLSI Design -BT24EC41O3A
2. Digital Electronics - BT24EC41O3B
3. Electronic Measurements and Instrumentations - BT24EC41O3C
4. Optical Communications - BT24EC41O3D

Pool 4: Open Elective 4 (Either of the 4 subjects)

1. Principles of Cellular & Mobile Communications - BT24EC41O4A
2. Fundamentals of Satellite Communications - BT24EC41O4B
3. Embedded Systems - BT24EC41O4C
4. Transducers and Signal Conditioning - BT24EC41O4D

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III Year-I Semester	ANALOG & DIGITAL IC APPLICATIONS (BT24EC3101)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Apply the operational principles and characteristics of op-amps to design and analyze analog circuits such as amplifiers and active filters.
- Design waveform generators and comparator circuits using op-amps for signal processing applications.
- To understand the concept of digital- to-analog, analog-to-digital circuit and its operation.
- Compare different data conversion techniques (DAC and ADC) and implement digital-to-analog and analog-to-digital conversion circuits in real-time applications.
- Implement and troubleshoot combinational and sequential logic circuits using digital ICs.
- Design and interface digital systems using programmable logic devices like PLDs and FPGAs.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	3	-	-	-	-	-	-	-	-	-	-	-
CO2	3	2	3	-	-	-	-	-	-	-	-	2	2	-
CO3	3	3	2	1	-	-	-	-	-	-	-	2	2	2
CO4	3	3	-	1	-	-	-	-	-	-	-	2	2	2
CO5	3	2	1	-	-	-	-	-	-	-	-	1	2	2
CO6	3	2	3	1	-	-	-	-	-	-	-	2	2	-

UNIT–I

Operational Amplifier: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, features of 741 Op-Amp, Modes of Operation-Inverting, Non- Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT-II

Op-Amp, IC-555 & IC565 Applications: Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, Waveform Generators – Triangular, Sawtooth, Square Wave, IC555 Timer-Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL-Block Schematic, principle and Applications.

UNIT-III

Data Converters: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs – Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.

UNIT-IV

Combinational Logic ICs: Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoders, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, De-multiplexers, Priority Generators/Checkers, Parallel Binary Adder/Subtractor, Magnitude Comparators.

UNIT-V

Sequential Logic IC's and Memories: Familiarity with commonly available 74XX & CMOS40XX Series ICs - All Types of Flip-flops, Synchronous Counters, Decade Counters, Shift Registers.

Memories - ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.

TEXTB OOKS:

1. Ramakanth A.Gayakwad-Op-Amps & Linear ICs, PHI,2003.
2. FloydandJain-DigitalFundamentals,8th Ed., Pearson Education,2005.

REFERENCE BOOKS:

1. D.Roy Chowdhury–Linear Integrated Circuits, New Age International(p) Ltd ,2nd Ed.,2003.
2. John.F.Wakerly–Digital Design Principles and Practices,3rd Ed., Pearson,2009.
3. Salivahana-Linear Integrated Circuits and Applications, TMH,2008.
4. WilliamD.Stanley-OperationalAmplifierswithLinearIntegratedCircuits,4th Ed., Pearson Education India, 2009.

e- Resources: -

- https://epgp.inflibnet.ac.in
- NPTEL Linear ICs, TI Op-Amp Handbook
- https://mrcet.com/downloads/digital_notes/EEE/13092021/LINEAR%20%26%20DIGITAL%20IC.pdf

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III Year-I Semester	DIGITAL COMMUNICATIONS (BT24EC3102)	L	T	P	C
		3	0	0	3

Course Outcomes:

- To Describe basic components of Digital Communication Systems and to determine the performance of different pulse digital modulation techniques.
- To determine the performance of digital modulation techniques for the generation and digital representation of the signals.
- To design optimum receiver for Digital Modulation techniques and to determine the probability of error for various digital modulation schemes.
- To analyze baseband receivers and design optimum receivers using matched filter concepts, and to evaluate the probability of error for coherent and non-coherent digital detection schemes.
- To compute and analyze error detecting and error correction codes block codes, cyclic codes.
- To compute and analyze convolution codes and Turbo codes.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	1	1	1
CO2	3	3	-	-	-	-	-	-	-	-	-	1	1	2
CO3	3	3	2	2	-	-	-	-	-	-	-	1	2	2
CO4	3	3	2	2	-	-	-	-	-	-	-	1	2	2
CO5	3	3	2	-	-	-	-	-	-	-	-	1	2	1
CO6	3	3	2	2	-	-	-	-	-	-	-	2	2	2

UNIT I

PULSE DIGITAL MODULATION: Elements of digital communication systems, advantages of digital communication systems, Elements of PCM: Sampling, Quantization & Coding, Quantization error, Companding in PCM systems. Differential PCM systems (DPCM). Delta modulation, its draw backs, adaptive delta modulation, comparison of PCM and DM systems, noise in PCM and DM systems, Time division multiplexing, Frequency division multiplexing.

UNIT II

DIGITAL MODULATION TECHNIQUES: Introduction, ASK, FSK, PSK, DPSK, DEPSK, QPSK, M-ary PSK, ASK, FSK, similarity of BFSK and BPSK.

UNIT III

DATA TRANSMISSION: Base band signal receiver, probability of error, the optimum filter, matched filter, probability of error using matched filter, coherent reception, non-coherent detection of FSK, calculation of error probability of ASK, BPSK, BFSK, QPSK.

UNIT IV

LINEAR BLOCK CODES: Introduction, Matrix description of Linear Block codes, Error detection and error correction capabilities of Linear block codes, Hamming codes, Binary cyclic codes, Algebraic structure, encoding, syndrome calculation, BCH codes

UNIT V

CONVOLUTION CODES: Introduction, encoding of convolution codes, time domain approach, transform domain approach. Graphical approach: state, tree and trellis diagram decoding using Viterbi algorithm, Turbo Codes.

TEXT BOOKS:

1. Digital communications - Simon Haykin, John Wiley, 2005.
2. Principles of Communication Systems – H. Taub and D. Schilling, TMH, 2003.
3. Digital Communications- J.Das, S.K.Mullick, P.K.Chatterjee, John willy & sons, 1986.

RERFERENCES:

1. Digital and Analog Communication Systems - Sam Shanmugam, John Wiley, 2005.
2. Digital Communications – John Proakis, TMH, 1983. Communication Systems Analog & Digital – Singh & Sapre, TMH, 2004.
3. Modern Analog and Digital Communication – B.P.Lathi, Oxford reprint, 3rd edition, 2004.

e- Resources:-

- https://nptel.ac.in/courses/108/105/108105093
- https://ocw.mit.edu/courses/6-450-principles-of-digital-communication-i-fall-2006/
- https://www.electronics-tutorials.ws/comm/

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III Year-I Semester	ANTENNAS AND WAVE PROPAGATION (BT24EC3103)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Identify basic antenna parameters.
- Quantify the fields radiated by various types of antennas.
- Design and analyze antenna arrays.
- Analyze radiation characteristics and performance of antenna arrays.
- Design and analyze wire antennas, loop antennas, reflector antennas, lens antennas, horn antennas and micro-strip antennas.
- Analyze antenna measurements to assess antenna's performance.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	1	1	1
CO2	3	3	-	2	-	-	-	-	-	-	-	1	2	2
CO3	3	3	3	2	-	-	-	-	-	-	-	1	2	2
CO4	3	3	2	2	-	-	-	-	-	-	-	1	2	2
CO5	3	3	3	2	2	-	-	-	-	-	-	1	3	3
CO6	3	3	2	3	2	-	-	-	-	-	-	2	2	2

UNIT-I:

ANTENNA FUNDAMENTALS: Introduction, Radiation Mechanism – Single Wire, 2-Wire, dipoles, Current Distribution on a thin wire antenna. Antenna Parameters - Radiation Patterns, Patterns in Principal Planes, Field Regions, Main Lobe and Side Lobes, Beam width, Radiation Intensity, Directivity, Antenna Efficiency, Gain, Beam Efficiency, Bandwidth, Polarization, Input Impedance, Beam Area and Resolution, Antenna Apertures, Aperture Efficiency, Effective Height, illustrated Problems.

UNIT-II:

THIN LINEAR WIRE ANTENNAS: Retarded Potentials, Radiation from Small Electric Dipole, Quarter wave Monopole and Half wave Dipole – Current Distributions, Evaluation of Field Components, Power Radiated, Radiation Resistance, Radiation Efficiency, Beam width, Directivity, Effective Area and Effective Height. Natural current distributions, fields and patterns of Thin Linear Center-fed Antennas of different lengths, Radiation Resistance at a point which is not current maximum, Antenna Theorems – Applicability and Proofs for equivalence of directional characteristics, Loop Antennas: Small Loops - Field Components, Comparison of far fields of small loop and short dipole, Concept of short magnetic dipole, D and R_r relations for small loops.

UNIT-III:

ANTENNA ARRAYS: 2 element arrays – different cases, Principle of Pattern Multiplication, N element Uniform Linear Arrays – Broadside, End-fire Arrays, EFA with Increased Directivity, Derivation of their characteristics and comparison; Concept of Scanning Arrays. Directivity Relations (no derivations), Related Problems. Binomial Arrays, Effects of Uniform and Non-uniform Amplitude Distributions, Design Relations Arrays with Parasitic Elements, Yagi-Uda Arrays, Folded Dipoles and their characteristics.

UNIT-IV

BROADBAND ANTENNAS: Log periodic antenna, Basic principle, Helical Antennas – Significance, Geometry, basic properties; Design considerations for monofilar helical antennas in Axial Mode and Normal Modes (Qualitative Treatment).

UHF AND MICROWAVE ANTENNAS:

Horn Antennas – Types, Optimum Horns, Design Characteristics of Pyramidal Horns; **Paraboloidal Reflectors**: – Geometry, characteristics, types of feeds, F/D Ratio, Spill Over, Back Lobes, Aperture Blocking, Off-set Feeds, Case grain Feeds.

Microstrip Antennas-Introduction, Features, Advantages and Limitations, Rectangular Patch Antennas –Geometry and Parameters, Impact of different parameters on characteristics, illustrated Problems.

UNIT-V

ANTENNA MEASUREMENTS: FRIIS Transmission Equation, Patterns Required, Set Up, Distance Criterion, Directivity and Gain Measurements (Comparison, Absolute and 3-Antenna Methods).

WAVE PROPAGATION: TYPES of propagations. Sky Wave Propagation – Formation of Ionospheric Layers and their Characteristics, Mechanism of Reflection and Refraction, Critical Frequency, MUF and Skip Distance; Space Wave Propagation – Mechanism, LOS and Radio Horizon, Field strength equation, illustrated Problems.

TEXT BOOKS:

1. Antenna Theory: Analysis And Design- Constantine A. Balanis, 3rd Edition, A John Wiley & Sons, Inc., Publication.
2. Antennas for All Applications – John D. Kraus and Ronald J. Marhefka, 3rd Edition, TMH, 2003.
3. Electromagnetic Waves and Radiating Systems – E.C. Jordan and K.G. Balmain, PHI, 2nd Edition, 2000.

REFERENCES:

1. Antennas and Wave Propagation-G.S.N. Raju, Pearson publications, 2006.
2. Transmission and Propagation – E.V.D. Glazier and H.R.L. Lamont, The Services Text Book of Radio, vol. 5, Standard Publishers Distributors, Delhi.
3. Antennas – John D. Kraus, McGraw-Hill, 2nd Edition, 1988.

e- Resources:-

- https://nptel.ac.in/courses/108/102/108102123
- https://ocw.mit.edu/courses/6-013-electromagnetics-and-applications-spring-2009/
- https://www.electronics-notes.com/articles/antennas-propagation/

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III Year I Semester	DIGITAL SYSTEM DESIGN THROUGH HDL (PE-I) (BT24EC31P1A)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the language constructs and programming fundamentals of Verilog HDL.
- Choose the suitable abstraction level for a particular digital design.
- Construct Combinational and sequential circuits in different modelling styles using Verilog HDL.
- Model digital circuits using dataflow and switch-level descriptions in Verilog HDL.
- Design and synthesize combinational and sequential logic circuits.
- Analyze and verify the functionality of digital circuits/systems using test benches.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	1	1	1	1
CO2	3	3	-	2	-	-	-	-	-	-	1	2	2	2
CO3	3	3	3	2	-	-	-	-	-	-	1	2	2	2
CO4	3	3	2	2	-	-	-	-	-	-	1	2	2	2
CO5	3	3	3	2	2	-	-	-	-	-	1	3	3	3
CO6	3	3	2	3	2	-	-	-	-	-	2	2	2	2

UNIT-I: Introduction to Verilog HDL and Gate Level Modelling:
Verilog as HDL, Levels of Design Description Basics of Concepts of Verilog, Data Types, System Task, Compiler directives, modules and ports. AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flipflops with Gate Primitives, Delay.

UNIT-II: Behavioural Modelling:
Introduction, structured processors, procedural assignments, timing controls, conditional statements, multi-way branching, loops, sequential and parallel blocks, generate blocks, Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in Behavioral model.

UNIT-III: Modelling at Data flow Level:
Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators, Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in dataflow model, Switch Level Modelling: Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitive delays.

UNIT-IV: FSM Design:

Functions, Tasks, User-defined, Primitives: Introduction, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines), Encoding Style: From Binary to One Hot. Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines.

UNIT-V: Components Test and Verification:

Test Bench – Combinational Circuits Testing, Sequential Circuits Testing, Test Bench Techniques, Design Verification, Assertion Verification.

Text Books:

1. Samir Palnitkar, "Verilog HDL A Guide to Digital and Synthesis" ,2nd Edition, Pearson Education,2006.

2. Michael, D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson Education India,2005.

Reference Books:

1. Padmanabhan, Tripura Sundari -Design through Verilog HDL, Wiley, 2016.
2. S. Brown, Zvonko – Vranesic, Fundamentals of Digital Logic with Verilog Design, TMH, 3rdEdision 2014.
3. J. Bhasker, A Verilog HDL Primer 2nd edition, BS Publications, 2001.

e- Resources:-

- https://nptel.ac.in/courses/108/105/108105132
- https://www.asic-world.com/verilog/index.html
- https://www.edaplayground.com/

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III Year-I Semester	OPTICAL COMMUNICATIONS (BT24EC31P1B)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Illustrate the optical fiber communication along with types of optical fibers.
- Identify various losses and dispersion models.
- Apply splicing techniques on fibers.
- Analyze different types of Optical sources, photo detectors for optical test equipment.
- Evaluate the power coupled in to optical fibers.
- Design optical system with budget analysis.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	-	-	-	-	-	-	-	-	-	-	-	3
CO2	3	3	-	-	-	-	-	-	-	-	-	-	-	3
CO3	3	3	-	-	-	-	-	-	-	-	-	-	-	3
CO4	3	3	-	-	-	-	-	-	-	-	-	-	-	3
CO5	3	3	-	-	-	-	-	-	-	-	-	-	-	3
CO6	-	3	1	2	-	-	-	-	-	-	-	-	-	3

UNIT I

Overview of optical fiber communication - Historical development, The general system, advantages of optical fiber communications. Optical fiber waveguides-Introduction, Ray theory transmission, Total Internal Reflection, Acceptance angle, Numerical Aperture, Skew rays, cylindrical fibers- Modes, V-number, Mode coupling, Step Index fibers, Graded Index fibers, Single mode fibers-Cutoff wavelength, Mode Field Diameter, Effective Refractive Index, Related problems.

UNIT II

Fiber materials: - Glass, Halide, Active glass, Chalgenide glass, Plastic optical fibers. Signal distortion in optical fibers-Attenuation, Absorption, Scattering and Bending losses, Core and Cladding losses, Information capacity determination, Group delay, Types of Dispersion: - Material dispersion, Wave-guide dispersion, Polarization-Mode dispersion, Intermodal dispersion, Pulse broadening in Graded index fiber, Related problems.

UNIT III

Optical fiber Connectors-Connector types, Single mode fiber connectors, Connector return loss, Fiber Splicing-Splicing techniques, Splicing single mode fibers, Fiber alignment and joint loss- Multimode fiber joints, single mode fiber joints.

UNIT IV

Optical sources-LEDs, Structures, Materials, Quantum efficiency, Power, Modulation, Power bandwidth product. Injection Laser Diodes- Modes, Threshold conditions, External quantum efficiency, Laser diode rate equations, Resonant frequencies, Reliability of LED&ILD, Optical detectors- Physical principles of PIN and APD, Detector response time, Comparison of Photo detectors, Related problems.

UNIT V

Source to fiber power launching - Output patterns, Power coupling, Power launching, Equilibrium Numerical Aperture, Laser diode to fiber coupling, Optical receiver operation- Fundamental receiver operation, Digital signal transmission, error sources, Receiver configuration, Digital receiver performance, Probability of Error, Quantum limit, Analog receivers. Optical system design - Point-to- point links- Component choice and considerations, Link power budget, Rise time budget with examples, Line coding in Optical links, WDM, Necessity, Principles, Measurement of Attenuation and Dispersion, Eye pattern.

TEXTBOOKS:

1. Optical Fiber Communications–Gerd Keiser, Mc Graw-Hill International edition,3rd Edition,2000.
2. Fiber Optic Communications– Joseph C.Palais, 4th Edition, Pearson Education, 2004.

RERFERENCES:

1. Fiber Optic Communications–D.K.Mynbaev, S.C.Gupta and Lowell L.Scheiner,PearsonEducation,2005.
2. Text Book on Optical Fiber Communication and its Applications–S.C.Gupta, PHI, 2005.
3. Fiber Optic Communication Systems–Govind P. Agarwal ,John Wiley, 3rd Ediition,2004.

e- Resources:-

- https://nptel.ac.in/courses/108/106/108106108
- https://ocw.mit.edu/courses/6-979-optical-communications-spring-2006/
- https://www.rp-photonics.com/optical_fiber_communications.html

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III Year I Semester	ELECTRONIC MEASUREMENTS AND INSTRUMENTATION (BT24EC31P1C)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the various Analog and Digital measuring Instruments.
- Aware of the principles and operations of various oscilloscopes.
- Learn measurements using DC bridges.
- Learn measurements using AC bridges.
- Familiarize different Signal Generators and function generators.
- Learn various transducers and intelligent sensors.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	-	-	-	-	-	-	-	1	1	1
CO2	3	2	2	2	-	-	-	-	-	-	-	1	1	1
CO3	3	1	1	1	-	-	-	-	-	-	-	1	1	-
CO4	3	3	1	1	-	-	-	-	-	-	-	1	1	-
CO5	3	1	1	1	-	-	-	-	-	-	-	1	1	1
CO6	3	2	2	2	-	-	-	-	-	-	-	1	1	1

UNIT I

Measuring Instruments: Introduction, Errors in Measurement, Accuracy, Precision, Resolution and Significant figures, Basic PMMC Meter- construction and working, DC and AC Voltmeters- Multirange, Range extension, DC Ammeter, Multimeter for Voltage, Current and resistance measurements.

Digital Instruments: Digital Voltmeters – Introduction, DVM's based on V–T, V–F and Successive approximation principles, Resolution and sensitivity, General specifications, Digital Multimeters, Digital frequency meters, Digital measurement of time.

UNIT II

Oscilloscopes: Introduction, Block diagram of CRO, Basic principle of CRT, CRT Construction and features, vertical amplifiers, horizontal deflection system- sweep, trigger pulse, delay line, sync selector circuits. Dual beam and dual trace CROs, Sampling and Digital storage oscilloscopes.

UNIT III

Bridges: DC Bridges for Measurement of resistance - Wheat stone bridge, Kelvin's Bridge, AC Bridges for Measurement of inductance- Maxwell's bridge, Hay's Bridge, Anderson bridge, Measurement of capacitance - Schearing Bridge, Wien Bridge, Errors and precautions in using bridges.

UNIT IV

Signal Generators: Introduction, Fixed and variable AF oscillator, Standard signal generator, Laboratory type signal generator, AF sine and Square wave generator, Function generator, Square and Pulse generator, Sweep frequency generator.

UNIT V

Transducers: Introduction, Types of Transducers, Electrical transducers, Selecting a transducer, Resistive transducer, Strain gauges, Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Temperature transducers-RTD, LVDT.

Intelligent Sensors: definition of intelligent instrumentation, types of instruments, Classification, Smart sensors, Cogent Sensors, Soft or Virtual sensors, Self-Adaptive Sensors, Self-Validating Sensors, Temperature Compensating Intelligent Sensors, Pressure Sensor, Indirect Sensing. (**Text Book 3**).

TEXT BOOKS

1. H. S. Kalsi, "Electronic Instrumentation", Third edition, Tata McGraw Hill, 2010.
2. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measurement Techniques", PHI, 6th Edition, 2010.
3. Manabendra Bhuyan, —Intelligent Instrumentation: Principles and Applications CRC Press, 2011.

REFERENCE BOOKS

1. A.K. Sawhney, Dhanpat Rai& Co., "A course in Electrical and Electronic Measurements and Instrumentation", 9th Edition, 2010.
2. David A. Bell, "Electronic Instrumentation & Measurements", PHI, 2nd Edition, 2006.

e- Resources:-

- https://nptel.ac.in/courses/108/106/108106146
- https://ocw.mit.edu/courses/res-6-010-electronic-measurements-spring-2004/
- https://www.electronics-tutorials.ws/measurement/

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III Year I Semester	COMPUTER ORGANIZATION AND ARCHITECTURE (BT24EC31P1D)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the representation of data, the register transfer language and Micro operations.
- Know the basic computer organization and design, programming the basic computer and design the micro programmer control unit.
- Know the development of central processing unit and explain various algorithms for computer arithmetic operations.
- Analyze CPU organization, instruction formats, addressing modes, and computer arithmetic algorithms.
- Interface various Peripheral devices and various data transfer operations.
- Study the memory Hierarchy and different types of memories.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-	3	2
CO2	3	2	2	-	-	-	-	-	-	-	-	-	3	2
CO3	3	2	2	-	-	-	-	-	-	-	-	-	3	2
CO4	3	2	2	1	-	-	-	-	-	-	-	-	3	2
CO5	3	2	2	1	-	-	-	-	-	-	-	-	3	2
CO6	3	2	2	1	-	-	-	-	-	-	-	-	3	2

UNIT-1 :

Introduction: Digital Computers, Von Neumann computers, Basic organization of a computer,

Data Representation: Data types, Complements, Fixed-point representation, Conversion of fractions, Floating-point representation.

Register Transfer and Micro operations: Register transfer language, Register transfer, Bus and Memory transfers, Arithmetic Micro operations, Logic Micro operations, Shift Micro operations, Arithmetic Logic Shift Unit.

UNIT-2

Basic Computer Organization and Design: Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference instructions, Input-Output and Interrupt, Complete Computer Description, Design of Basic computer.

Programming the Basic Computer: Introduction, Machine Language, Assembly language, The Assembler, Program Loops, Programming Arithmetic and Logic Operations.

Micro programmed Control: Control Memory, Address Sequencing, Micro program Example, Design of Control Unit (**Preferably from Reference Book 2**).

UNIT-3

Central Processing Unit: Introduction, General Register Organization, Stack organization, Instruction Formats, Addressing Modes, Data transfer and Manipulation, Program Control, Reduced Instruction Set Computer.

Computer Arithmetic: Introduction, Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating-Point Arithmetic Operations, Decimal Arithmetic Unit, Decimal Arithmetic Operations.

UNIT – 4

Input-Output organization: Peripheral Devices, Input-Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor (IOP), Serial Communication.

UNIT– 5

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware.

Text Book

1. M. Morris Mano," Computer System Architecture," Pearson Publishers, Revised Third Edition

Reference Books

1. John P Hayes, "Computer Architecture and Organization,"Mc-Graw Hill Publishers, Third Edition.
2. Carl Hamacher, "Computer Organization," Tata Mc-Graw Hill Publishers, Fifth Edition.

e- Resources:-

- https://nptel.ac.in/courses/106/103/106103068
- https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/
- https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/

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III Year I Semester	ELECTRONIC DEVICES AND CIRCUITS (BT24EC31O1A)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Apply the basic concepts of semiconductor physics.
- Understand the formation of p-n junction and how it can be used as a p-n junction as diode in different modes of operation.
- Analyze the construction, working principle of Semiconductor Devices and Diode Circuits.
- Know the need of transistor biasing, various biasing techniques for BJT and FET and stabilization concepts with necessary expressions.
- Apply small signal low frequency transistor amplifier circuits using BJT and FET in different configurations.
- Understand the working of MOSFETs in digital circuits.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	-	-	-	-	2	1	-	-	-	3	1	-
CO2	3	1	1	-	-	-	2	1	-	-	-	3	2	-
CO3	3	1	-	1	-	-	2	1	-	-	-	3	2	-
CO4	3	1	-	-	-	-	2	1	-	-	-	3	2	-
CO5	3	1	-	-	-	-	2	1	-	-	-	3	2	-
CO6	3	1	1	-	-	-	2	1	-	-	-	3	2	-

UNIT-I:

Review of Semi-Conductor Physics: Hall effect, continuity equation, law of junction, Fermi Dirac function, Fermi level in intrinsic and extrinsic Semiconductors.

Junction Diode Characteristics: Energy band diagram of PN junction Diode, Open circuited p-n junction, Biased p-n junction, p-n junction diode, current components in PN junction Diode, diode equation, V-I Characteristics, temperature dependence on V-I characteristics, Diode resistance, Diode capacitance.

UNIT-II:

Special Semiconductor Devices: Zener Diode, Breakdown mechanisms, Zener diode applications, LED, Varactor Diode, Photodiode, Tunnel Diode, UJT, PNPN Diode, SCR. Construction, operation and V-I characteristics.

Rectifiers and Filters: Basic Rectifier setup, half wave rectifier, full wave rectifier, bridge rectifier, derivations of characteristics of rectifiers, rectifier circuits-operation, input and output waveforms, Filters, Inductor filter (Series inductor), Capacitor filter (Stunt inductor), π-Filter, comparison of various filter circuits in terms of ripple factors.

UNIT- III: Transistor Characteristics:

BJT: Junction transistor, transistor current components, transistor equation, transistor configurations, transistor as an amplifier, characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, Ebers-Moll model of a transistor, punch through/ reach through, Photo transistor, typical transistor junction voltage values.

FET: FET types, construction, operation, characteristicsμ, g_m, $r_d$parameters, MOSFET-types, construction, operation, characteristics, comparison between JFET and MOSFET.

UNIT- IV: Transistor Biasing and Thermal Stabilization: Need for biasing, operating point, load line analysis, BJT biasing- methods, basic stability, fixed bias, collector to base bias, self-bias, Stabilization against variations in V_{BE}, Ic, and β, Stability factors, (S,S',S"), Bias compensation, Thermal runaway, Thermal stability. FET Biasing- methods and stabilization.

UNIT- V: Small Signal Low Frequency Transistor Amplifier Models:

BJT: Two port network, Transistor hybrid model, determination of h-parameters, conversion of h-parameters, generalized analysis of transistor amplifier model using h-parameters, Analysis of CB, CE and CC amplifiers using exact and approximate analysis, Comparison of transistor amplifiers.

FET: Generalized analysis of small signal model, Analysis of CG, CS and CD amplifiers, comparison of FET amplifiers.

Text Books:

1. Electronic Devices and Circuits- J. Millman, C. Halkias, Tata Mc-Graw Hill, SecondEdition,2007.
2. Electronic Devices and Circuits by David A. Bell, Oxford University Press.
3. Electronics devices & circuit theory-Robert L.Boylestad and LouiNashelsky, Pearson/ Prentice Hall, tenth edition,2009.

References:

1. Integrated Electronics-J. Millman, C. Halkias,Tata Mc-Graw Hill, Second Edition,2009
2. Electronic Devices and Circuits-K. Lal Kishore, BS Publications, Fourth Edition,2016.

e- Resources: -

- https://nptel.ac.in/courses/108/105/108105112
- https://ocw.mit.edu/courses/6-012-microelectronic-devices-and-circuits-fall-2009/
- https://www.electronics-tutorials.ws/amplifier/

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III Year I Semester	SIGNALS AND SYSTEMS (BT24EC31O1B)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Differentiate the various classifications of signals and systems.
- Analyze the frequency domain representation of signals using Fourier concepts.
- Classify the systems based on their properties and determine the response of LTI Systems.
- Perform linear convolution and understand its implications on system output.
- Know the sampling process and various types of sampling techniques.
- Apply Laplace and z-transforms to analyze signals and Systems (continuous & discrete).

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-	2	2
CO2	3	3	-	-	2	-	-	-	-	-	-	-	2	1
CO3	3	3	-	2	2	-	-	-	-	-	-	-	-	-
CO4	3	3	-	2	2	-	-	-	-	-	-	-	-	-
CO5	3	3	-	2	2	-	-	-	-	-	-	-	1	1
CO6	3	3	3	-	2	-	-	-	-	-	-	-	2	1

UNIT- I: INTRODUCTION: Definition of Signals and Systems, Classification of Signals, Classification of Systems, Operations on signals: time-shifting, time-scaling, amplitude-shifting, amplitude-scaling. Problems on classification and characteristics of Signals and Systems, Complex exponential and sinusoidal signals, Singularity functions and related functions: impulse function, step function signum function and ramp function.

UNIT–II: FOURIER SERIES AND FOURIER TRANSFORM:
Fourier series representation of continuous time periodic signals, Dirichlet's conditions, Trigonometric Fourier series and Exponential Fourier series, Relation between Trigonometric and Exponential Fourier series, Complex Fourier spectrum. Deriving Fourier transform from Fourier series, Fourier transform of standard signals, properties of Fourier transforms, Fourier transforms involving impulse function and Signum function. Related problems.

UNIT-III:

CORRELATION: Auto-correlation and cross-correlation of functions, properties of correlation function, Energy density spectrum, Parseval's theorem, Power density spectrum, Relation between Convolution and correlation, Detection of periodic signals in the presence of noise by correlation. **SAMPLING THEOREM:** Graphical and analytical proof or Band Limited Signals, impulse sampling, Natural and Flat top Sampling, Reconstruction of signal from its samples, Aliasing, Related problems.

UNIT–IV:

LAPLACE TRANSFORMS: Introduction, Concept of region of convergence (ROC) for Laplace transforms, constraints on ROC for various classes of signals, Properties of L.T's, Inverse Laplace transform, Relation between L.T's, and F.T. of a signal. Laplace transform of certain signals using waveform synthesis.

UNIT–V:

Z–TRANSFORMS: Concept of Z-Transform of a discrete sequence. Region of convergence in Z-Transform, constraints on ROC for various classes of signals, Inverse Z-transform, properties of Z-transforms, Distinction between Laplace, Fourier and Z transforms.

TEXT BOOKS:

1. Signals, Systems & Communications-B.P. Lathi, BSPublications,2003.
2. Signals and Systems-A.V. Oppenheim, A.S. Willsky and S.H. Nawab, PHI,2ndEdn,1997.
3. Signals & Systems-Simon Haykin and VanVeen, Wiley,2ndEdition,2007.

REFERENCE BOOKS:

1. Principles of Linear Systems and Signals–BP Lathi, Oxford UniversityPress,2015
2. Signals and Systems–TK Rawat, Oxford University press,2011.

e- Resources: -

- https://nptel.ac.in/courses/108/101/108101037
- https://ocw.mit.edu/courses/6-003-signals-and-systems-fall-2011/
- https://www.allaboutcircuits.com/technical-articles/subjects/signals-and-systems/

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III Year I Semester	PROBABILITY THEORY AND RANDOM VARIABLES (BT24EC3101C)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Analyze key distributions like Binomial, Poisson, Gaussian, and Exponential.
- Perform operations on single and multiple Random variables.
- Determine the Spectral and temporal characteristics of Random Signals.
- Compute autocorrelation and cross-correlation functions.
- Characterize LTI systems driven by stationary random process by using ACFs and PSDs.
- Understand the concepts of Noise and Information theory in Communication systems.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	-
CO2	-	-	3	-	-	-	-	-	-	-	-	-	-	2
CO3	-	-	3	-	-	-	-	-	-	-	-	-	2	-
CO4	-	3	-	-	-	-	-	-	-	-	-	-	2	-
CO5	-	3	-	-	-	-	-	-	-	-	-	-	-	2
CO6	-	3	-	-	-	-	-	-	-	-	-	-	-	2

UNIT I

THE RANDOM VARIABLE: Introduction, Review of Probability Theory, Definition of a Random Variable, Conditions for a Function to be a Random Variable, Discrete, Continuous and Mixed Random Variables, Distribution and Density functions, Properties, Binomial, Poisson, Uniform, Gaussian, Exponential, Rayleigh, Conditional Distribution, Conditional Density, Properties.

UNIT II

OPERATION ON ONE RANDOM VARIABLE - EXPECTATIONS: Introduction, Expected Value of a Random Variable, Function of a Random Variable, Moments about the Origin, Central Moments, Variance and Skew, Chebychev's Inequality, Characteristic Function, Moment Generating Function, Transformations of a Random Variable: Monotonic Transformations for a Continuous Random Variable, Non-monotonic Transformations of Continuous Random Variable.

UNIT III

MULTIPLE RANDOM VARIABLES: Vector Random Variables, Joint Distribution Function, Properties of Joint Distribution, Marginal Distribution Functions, Conditional Distribution and Density, Statistical Independence, Sum of Two Random Variables, Sum of Several Random Variables, Central Limit Theorem: Unequal Distribution, Equal Distributions.

OPERATIONS ON MULTIPLE RANDOM VARIABLES: Joint Moments about the Origin, Joint Central Moments, Joint Characteristic Functions, Jointly Gaussian Random Variables: Two Random Variables case, N Random Variables case, Properties, Transformations of Multiple Random Variables, Linear Transformations of Gaussian Random Variables.

UNIT IV

RANDOM PROCESSES – TEMPORAL CHARACTERISTICS: The Random Process Concept, Classification of Processes, Deterministic and Nondeterministic Processes, Distribution and Density Functions, Concept of Stationarity and Statistical Independence. First-Order Stationary Processes, Second-order and Wide-Sense Stationarity, N^{th}-order and Strict -Sense Stationarity, Time Averages and Ergodicity, Autocorrelation Function and its Properties, Cross- Correlation Function and its Properties, Covariance Functions, Gaussian Random Processes, Poisson Random Process.

UNIT V

RANDOM PROCESSES - SPECTRAL CHARACTERISTICS: The Power Density Spectrum: Properties, Relationship between Power Density Spectrum and Autocorrelation Function, The Cross-Power Density Spectrum, Properties, Relationship between Cross-Power Density Spectrum and Cross-Correlation Function.

LINEAR SYSTEMS WITH RANDOM INPUTS: Random Signal Response of Linear Systems: System Response – Convolution, Mean and Mean-squared Value of System Response, Autocorrelation Function of Response, Cross-Correlation Functions of Input and Output, Spectral Characteristics of System Response: Power Density Spectrum of Response, Cross-Power Density Spectra of Input and Output, Band pass, Band-Limited and Narrowband Processes, Properties.

TEXT BOOKS:

1. Probability, Random Variables & Random Signal Principles, Peyton Z. Peebles, TMH, 4^{th} Edition, 2001.
2. Probability, Random Variables and Stochastic Processes, Athanasios Papoulis and S.Unni krisha, PHI, 4^{th} Edition, 2002.
3. Probability Theory and Stochastic Processes – B. Prabhakara Rao, BS Publications.

REFERENCE BOOKS:

1. Probability and Random Processes with Applications to Signal Processing, Henry Stark and John W. Woods, Pearson Education, 3rd Edition.
2. Schaum's Outline of Probability, Random Variables, and Random Processes.
3. An Introduction to Random Signals and Communication Theory, B.P. Lathi, International Textbook, 1968.
4. Probability Theory and Random Processes, P. Ramesh Babu, McGrawHill, 2015.

e- Resources: -

- https://nptel.ac.in/courses/108/106/108106083
- https://ocw.mit.edu/courses/6-041-probabilistic-systems-analysis-and-applied-probability-fall-2010/

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III Year I Semester	NETWORK ANALYSIS (BT24EC31O1D)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Identify basic electrical circuits with nodal and mesh analysis and Apply network theorems for the analysis of AC and DC networks.
- Analyze transient response and Steady state response of network.
- Apply nodal and mesh networks, series and parallel circuits, steady state response, different circuit topologies (with R, L and C components).
- Apply steady state response, different circuit topologies (with R, L and C components).
- Analyze the resonant circuits and draw the locus diagrams.
- Develop the parameters of a two-port network.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	-	-	-	-	-	-	2	-	2
CO2	3	3	2	2	1	-	-	-	-	-	-	2	-	2
CO3	3	3	2	2	1	-	-	-	-	-	-	2	-	2
CO4	3	2	2	1	1	-	-	-	-	-	-	2	-	2
CO5	3	2	2	2	1	-	-	-	-	-	-	2	-	2
CO6	3	1	2	2	2	-	-	-	-	-	-	2	-	2

UNIT – I

Introduction to Electrical Circuits: Network elements classification, Electric charge and current, Electric energy and potential, Resistance parameter – series and parallel combination, Inductance parameter – series and parallel combination, Capacitance parameter – series and parallel combination. Energy sources: Ideal, Non-ideal, Independent and dependent sources, Source transformation, Kirchoff's laws, Mesh analysis and Nodal analysis problem solving with resistances only including dependent sources also.

Definitions of terms associated with periodic functions: Time period, Angular velocity and frequency, RMS value, Average value, Form factor and peak factor- problem solving, Phase angle, Phasor representation, Addition and subtraction of phasors, mathematical representation of sinusoidal quantities, explanation with relevant theory, problem solving. Principal of Duality with examples

Definitions of branch, node, tree, planar, non-planar graph, incidence matrix, basic tie set schedule, basic cut set schedule.

UNIT – II

Transients : First order differential equations, Definition of time constants, R-L circuit, R-C circuit with DC excitation, Evaluating initial conditions procedure, second order differential equations, homogeneous, non-homogenous, problem solving using R-L-C elements with DC excitation and AC excitation, Response as related to s-plane rotation of roots. Solutions using Laplace transform method.

UNIT – III

Steady State Analysis of A.C Circuits: Impedance concept, phase angle, series R-L, R-C, R-L-C circuits problem solving. Complex impedance and phasor notation for R-L, R-C, R-L-C problem solving using mesh and nodal analysis, Star-Delta conversion, problem solving.

Coupled Circuits: Coupled Circuits: Self inductance, Mutual inductance, Coefficient of coupling, analysis of coupled circuits, Natural current, Dot rule of coupled circuits, conductively coupled equivalent circuits- problem solving.

UNIT – IV Resonance: Introduction, Definition of Q, Series resonance, Bandwidth of series resonance, Parallel resonance, Condition for maximum impedance, current in anti resonance, Bandwidth of parallel resonance, general case-resistance present in both branches, anti resonance at all frequencies.

Network Theorems: Thevinin's, Norton's, Milliman's, Reciprocity, Compensation, Substitution, Superposition, Max Power Transfer, Tellegens- problem solving using dependent sources also

UNIT – V Two-port Networks: Relationship of two port networks, Z-parameters, Y-parameters, Transmission line parameters, h-parameters, Inverse h-parameters, Inverse Transmission line parameters, Relationship between parameter sets, Parallel connection of two port networks, Cascading of two port networks, series connection of two port networks, problem solving including dependent sources also.

TEXT BOOKS:

1. Network Analysis – ME Van Valkenburg, Prentice Hall of India, 3rd Edition, 2000.
2. Network Analysis by K.Satya Prasad and S Sivanagaraju, Cengage Learning.
3. Electric Circuit Analysis by Hayt and Kimmarle, TMH.

REFERENCES:

1. Network lines and Fields by John. D. Ryder 2nd edition, Asia publishing house.
2. Basic Circuit Analysis by DR Cunninghan, Jaico Publishers.
3. Network Analysis and Filter Design by Chadha, Umesh Publications.

e- Resources: -

- https://www.allaboutcircuits.com/textbook/alternating-current/
- https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/
- https://nptel.ac.in/courses/108/106/108106073

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III Year-I Semester	ANALOG AND DIGITAL IC APPLICATIONS LAB (BT24EC3104)	L	T	P	C
		0	0	3	1.5

PART-A: (Minimum **SIX** Experiments to be conducted):

1. OP AMP Applications – Adder, Subtractor, Comparator Circuits.
2. Integrator and Differentiator Circuits using IC 741.
3. Active Filter Applications – LPF, HPF (first order)
4. Active Filter Applications – BPF, Band Reject (Wideband) and Notch Filters.
5. IC 741 Oscillator Circuits – Phase Shift and Wien Bridge Oscillators.
6. Function Generator using OP AMPs.
7. IC 555 Timer – Astable & Mono-stable Operation Circuit.
8. Schmitt Trigger Circuits – using IC 741 and IC 555.
9. IC 565 – PLL Applications.
10. IC 566 – VCO Applications.
11. 4 bit DAC using OP AMP.

Equipment required for Laboratories:

1. RPS
2. CRO
3. Function Generator
4. Multi Meters
5. IC Trainer Kits (Optional)
6. Bread Boards
7. Components: - IC741, IC555, IC565, IC1496, IC723, 7805, 7809, 7912 etc.
8. Analog IC Tester

PART-B: (Minimum **SIX** Experiments to be conducted):

The students are required to design and draw the internal structure of the following Digital Integrated Circuits and to develop HDL (VHDL, Verilog HDL) source code, perform simulation using relevant simulator and analyze the obtained simulation results using appropriate synthesizer. Further, it is required to verify the logic with necessary hardware.

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List of Experiments:

1. Realization of Logic Gates
2. 3 to 8 Decoder- 74138
3. 8*1 Multiplexer-74151 and 2*1 De-multiplexer-74155
4. 4-Bit Comparator-7485.
5. D Flip-Flop- 7474
6. Decade Counter- 7490
7. Universal shift register-74194/195
8. RAM (16*4)-74189 (read and write operations)

Equipment Required:

1. Xilinix Vivado/Equivalent Standard IDE
2. Personal computer with necessary peripherals
3. Hardware kits- Various FPGA families.

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III Year I Semester	ANALOG AND DIGITAL COMMUNICATIONS LAB (BT24EC3105)	L	T	P	C
		0	0	3	1.5

List of Experiments:

(Fourteen experiments to be done-**The students have to calculate the relevant parameters**)–
(a. Hardware, b. MATLAB Simulink c. MATLAB Communication toolbox)

Part-A

1. Amplitude Modulation-Modulation & Demodulation.
2. AM-DSBSC-Modulation & Demodulation.
3. Diode Detector.
4. Pre-emphasis & De-emphasis.
5. Frequency Modulation-Modulation & Demodulation.
6. Verification of Sampling Theorem.
7. Pulse Amplitude Modulation & Demodulation.
8. PWM, PPM–Modulation & Demodulation.

Part-B

1. Time division multiplexing.
2. Frequency Division Multiplexing.
3. Pulse code modulation.
4. Differential pulse code modulation.
5. Delta modulation.
6. Frequency shift keying.
7. Phase shift keying.
8. Differential phase shift keying.
9. Companding.
10. Source Encoder and Decoder.
11. Linear Block Code-Encoder and Decoder and Binary Cyclic Code–Encoder and Decoder.
12. Convolution Code–Encoder and Decoder.

Note: All the above experiments are to be executed/completed using hardware boards and also to be simulated on Mat lab.

Equipment & Software required: Software:

i) Computer Systems with latest specifications ii) Connected in LAN(Optional)
iii) Operating system (Windows/Linux software) iv) Simulations software (Simulink &MATLAB)

Equipment:

i. RPS -0 –30V
ii. CRO -0–20MHz.
iii. Function Generators -0–1MHz
iv. Components and Breadboards
v. Multi meters and other meters

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III Year-I Semester	APPLICATIONS OF LAB VIEW FOR INSTRUMENTATION & COMMUNICATIONS (BT24EC3106)	L	T	P	C
		0	1	2	2

Course Outcomes:

- Develop loops, case structures, arrays, and clusters.
- Realize real time applications using NI DAQ hardware.
- Implement Coding techniques using LabVIEW.
- Design automation and process control application.
- Apply LabVIEW for data processing applications.

Unit I:

Introduction to LabVIEW & Virtual Instrumentation: Overview of LabVIEW: Graphical programming paradigm, LabVIEW Environment: Front panel, block diagram, data flow programming, Creating simple Virtual Instruments (VIs), Debugging and troubleshooting techniques, Implementing loops, case structures, arrays, and clusters.

Unit II:

Data Acquisition & Signal Processing: Interfacing sensors (temperature, pressure, light, etc.) with LabVIEW, Real-time data acquisition using NI DAQ hardware, Signal generation: Sine, Square, Triangular waves, Fourier Transform (FFT) for frequency analysis, Filtering techniques: Low-pass, High-pass, Band-pass filters.

Unit III:

Communication System Implementation: AM and FM Modulation/Demodulation using LabVIEW, Simulation of Digital Modulation Schemes (ASK, PSK, FSK), Eye diagrams and constellation plots for digital signals, Error detection and correction: Parity, CRC, Hamming Code.

Unit IV: Instrumentation & Automation Applications:

Real-time data logging and file handling (Excel/CSV), PID Controller Design for automation and process control, Motor speed control using LabVIEW and DAQ, Signal visualization and user interface design.

Unit V: Advanced Applications:

Image Processing using LabVIEW, Wireless communication using Bluetooth & Wi-Fi in LabVIEW, IoT Integration-Cloud-based monitoring and remote data access, Project-based learning-

Textbooks & References

1. R. W. Larsen, LabVIEW for Engineers, 1st ed., Prentice Hall, 2011.
2. G. W. Johnson and R. Jennings, LabVIEW Graphical Programming, 4th ed., McGraw-Hill, 2017.
3. National Instruments, "LabVIEW Tutorials & Documentation," Available: https://www.ni.com.J. Jerome, Virtual Instrumentation Using LabVIEW, 1st ed., PHI Learning Pvt

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III Year-I Semester	DESIGN OF PCB & ANTENNAS LAB (BT24EC3107)	L	T	P	C
		0	0	2	1

Merits of PCB Machine:

1. CNC based for Better Accuracy and results.
2. Etching, Engraving and Drilling can be done with same Machine.
3. Maintenance free machine compared to chemical method.
4. Compatible with multiple software Gerber / G code.
5. Reduction of time and Inventory.
6. Height mapping for bed level and depth sensing.
7. Surface mapping of bed.
8. Power Optimized system ability to run on ups systems unlike other Machines.
9. High precision lead screw.
10. 5umeter resolution, 0.001 repeatability, 2 layers with FR4.
11. Scalability from a single prototype to a batch of 10-50 PCBs.

Scope of learning:

1. In house PCB proto type manufacturing process.
2. How to convert simulation results into real time Electronic boards/ Projects.
3. Designing according to project requirements.
4. Along with PCB other Multi materials support carbon fiber sheets, Drone frames, Engraved
5. Acrylic sheets. Engraving on aluminium.
6. Latest multi domain projects extension 3D printing and Additive Manufacturing.
7. Exposure to design the proto type products.

ANTENNAS LAB:

List of experiments: (Any Ten experiments using any simulation software)

1. Generation of EM-Wave.
2. Impedance Matching using Smith Chart.
3. Calculation of phase and group velocity calculation.
4. Plot of Radiation pattern of dipole antenna.
5. Plot of Radiation pattern of monopole antenna.
6. Plot of Radiation pattern of Uniform Linear Array.
7. Measurement of radiation pattern of all wired and aperture antennas.
8. Measurement of radiation pattern of planar antennas.

9. Measurement of radiation pattern of reflector antennas.
10. Measurement of radiation pattern of array antennas.
11. Analysis of co-polarization and cross polarization.
12. Performance analysis of Yagi -Uda antenna.
13. Performance analysis of Helix antenna.
14. Radio wave propagation path loss calculations.

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III Year II Semester	VLSI DESIGN (BT24EC3201)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
- Design MOSFET based logic circuit.
- Design basic building blocks in Analog IC design.
- Apply VLSI design principles to implement CMOS, analog, and FPGA-based digital systems.
- Design various CMOS logic circuits for design of Combinational logic circuits.
- Analyze the behavior of static and dynamic logic circuits.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	1	1	-	-	-	-	-	-	2	1
CO2	3	3	2	2	1	1	-	-	-	-	-	-	2	2
CO3	3	3	2	2	1	1	-	-	-	-	-	-	2	2
CO4	3	3	3	3	2	2	1	1	-	-	-	-	2	3
CO5	3	3	3	2	2	2	1	1	-	-	-	-	2	3
CO6	3	3	2	2	1	1	-	-	-	-	-	-	2	2

UNIT-I:

INTRODUCTION AND BASIC ELECTRICAL PROPERTIES OF MOS CIRCUITS: VLSI Design Flow, Introduction to IC technology, Fabrication process: nMOS, pMOS and CMOS. I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit. nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, and through one or more pass transistors. Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and BiCMOS technology, MOS Layers, Stick Diagrams, Design Rules and Layout, Layout Diagrams for MOS circuits.

UNIT-II:

BASIC CIRCUIT CONCEPTS: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, some area Capacitance Calculations, The Delay Unit, Inverter Delays, driving large capacitive loads, Propagation Delays, Wiring Capacitances, Choice of layers.

SCALING OF MOS CIRCUITS: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise and current density.

UNIT-III:

BASIC BUILDING BLOCKS OF ANALOG IC DESIGN: Regions of operation of MOSFET, Modelling of transistor, body bias effect, biasing styles, single stage amplifier with resistive load, single stage amplifier with diode connected load, Common Source amplifier, Common Drain amplifier, Common Gate amplifier, current sources and sinks.

UNIT-IV:

CMOS COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUIT DESIGN:

Static CMOS Design: Complementary CMOS, Rationed Logic, Pass-Transistor Logic, design of Half adder, full adder, multiplexer, decoder. **Dynamic CMOS Design:** Dynamic Logic-Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Design examples of sequential circuits: Cross coupled NAND and NOR flipflops, D flipflop, SR JK flip flop, SR Master Slave flip flop.

UNIT-V:

FPGA DESIGN: FPGA design flow, Basic FPGA architecture, FPGA Technologies, Introduction to FPGA Families.

INTRODUCTION TO ADVANCED TECHNOLOGIES: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET.

TEXTBOOKS:

1. Essentials of VLSI Circuits and Systems - Kamran Eshraghian, Douglas and A. Pucknell.
2. And Sholeh Eshraghian, Prentice-Hall of India Private Limited, 2005 Edition.
3. Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw Hill, 2003.
4. Digital Integrated Circuits, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, 2nd edition,2016.

REFERENCES:

1. "Introduction to VLSI Circuits and Systems", John P. Uyemura, John Wiley & Sons, reprint 2009.
2. Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies Vinod Kumar Khanna, Springer India, 1st edition, 2016.
3. FinFETs and other multi-gate transistors, ColingeJP, Editor New York, Springer,2008.

e- Resources: -

- https://nptel.ac.in/courses/117/106/117106092
- https://ocw.mit.edu/courses/6-012-microelectronic-devices-and-circuits-spring-2009/
- https://www2.eecs.berkeley.edu/Courses/EE141/

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III Year- II Semester	MICROPROCESSOR AND MICROCONTROLLERS (BT24EC3202)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the architecture of 8086 microprocessor and their modes of operation.
- Demonstrate various addressing modes and assembly language programming for 8086 microprocessors.
- Analyze interfacing of 8086 microprocessors with different Peripherals.
- To design and develop the new interface ideas in real time applications.
- Demonstrating the architecture of 8051 Microcontrollers, its instruction set and interfacing with different peripherals.
- Understand the features and instruction set of ARM Processor.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	-	-	-	-	-	1
C02	2	2	-	-	-	-	-	-	-	-	-	-	-	1
CO3	2	2	2	-	-	-	-	-	-	-	-	-	-	2
CO4	2	2	2	-	-	-	-	-	-	-	-	-	-	2
CO5	2	1	-	-	-	-	-	-	-	-	-	-	-	2
CO6	2	2	2	-	-	-	-	-	-	-	-	-	-	2

Unit –I Introduction: Basic Microprocessor architecture, Harvard and Von Neumann architectures with examples, Microprocessor Unit versus Microcontroller Unit, History and classifications of Microprocessor and Microcontroller.
8086 Architecture: register organization, internal architecture of 8086, pin description of 8086, minimum mode and maximum mode of 8086 operation and timing diagrams.

Unit –II 8086 Programming: instruction set, addressing modes, assembler directives, programming with an assembler, writing simple programs with an assembler, stack and stack structure, interrupts and interrupt service routines 8086 system,

Unit –III 8086 Interfacing: Semiconductor memories interfacing (RAM, ROM), Intel 8255 programmable peripheral interface, Interfacing switches and LEDS, Interfacing seven segment displays, Intel 8251 USART architecture and interfacing, Intel 8237a DMA controller, stepper motor, A/D and D/A converters, Need for 8259 programmable interrupt controllers.

Unit –IV Intel 8051 Microcontroller and Interfacing

Architecture, Hardware concepts, Input/output ports and circuits, external memory, counters/timers, serial data input/output, interrupts. Assembly language programming: Instructions, addressing modes, simple programs. Interfacing to 8051: A/D and D/A Convertors, Stepper motor interface, keyboard, LCD Interfacing, Traffic light control.

Unit –V ARM Architectures and Processors:

Introduction to CISC and RISC architectures, ARM Architecture, ARM Processors Families, ARM Cortex-M Series Family, ARM Cortex-M3 Processor Functional Description, Instruction set summary, System address map, write buffer, bit-banding. Programmers Model – Modes of operation and execution, stack pointer, exceptions and interrupt handling.

ARM Cortext-M3 programming – Software delay, Programming techniques, Loops, Stack and Stack pointer, subroutines and parameter passing, parallel I/O, Nested Vectored Interrupt Controller– functional description and NVIC programmers' model.

TEXT BOOKS:

1. Advanced microprocessors and peripherals by K. M. Bhurchandi, A. K. Ray 3e
2. The 8051 Microcontrollers and Embedded systems Using Assembly and C, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D.McKinlay; Pearson 2-Edition,2011.
3. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu., Newnes Third edition.

REFERENCE BOOKS:

1. Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers: A Practical Approach in English, by Dr. Alexander G. Dean, Published by Arm EducationMedia,2017.
2. Cortex-M3Technical Reference Manual.

e- Resources: -

- https://nptel.ac.in/courses/108/108/108108117
- https://www.electronics-tutorials.ws/microcontroller/8051.html
- https://www.keil.com/cortex-m3/

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III Year II Semester	DIGITAL SIGNAL PROCESSING (BT24EC3203)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the concepts of discrete signals and discrete systems with its characteristics.
- Calculate z-Transform, Fourier Transform, Discrete Fourier Transform of discrete signals.
- Understand the algorithms for the efficient computation of DFT coefficients of signals.
- Analyze and design discrete-time signal processing algorithms using transform and filtering techniques.
- Design the FIR and IIR filters.
- Know the architectures of various DSP processors and its addressing modes, assembly language instructions.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO 2
CO1	3	2	1	1	1	-	-	-	-	-	-	-	2	1
C02	3	2	1	1	1	-	-	-	-	-	-	-	2	1
CO3	3	2	1	1	1	-	-	-	-	-	-	-	2	1
CO4	3	3	2	2	1	1	1	-	-	-	-	-	2	2
CO5	3	3	2	2	1	1	1	-	-	-	-	-	2	2
CO6	3	3	2	2	2	2	1	1	-	-	-	-	2	2

UNIT-1:

Introduction: Signals, Systems, and Signal Processing, Classification of Signals, The Concept of Frequency in Continuous Time and Discrete Time Signals

Discrete Time Signals and Systems: Discrete Time Signals, Discrete Time Systems, Analysis of Discrete Time Linear Time Invariant Systems, Discrete Time Systems Described by Difference Equations, Implementation of Discrete Time Systems, Correlation of Discrete Time Signals.

Frequency Analysis of Signals: Frequency Analysis of Continuous Time Signals, Frequency Analysis of Discrete Time Signals, Frequency Domain and Time Domain Signal Properties, Properties of the Fourier Transform for Discrete Time Signals. **Frequency Domain Analysis of LTI Systems:** Frequency domain characteristics of LTI systems, Frequency response of LTI systems.

UNIT-2:

The z-Transform and Its Applications to the Analysis of LTI Systems: The z-Transform, Properties, Rational z Transforms, Inversion of the z-Transform, Analysis of Linear Time Invariant Systems in the z-Domain, The One sided z-Transform. **(Review only for entirez – Transform topic).**

The Discrete Fourier Transform: Its Properties and Applications: Frequency Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT, Frequency Analysis of Signals Using DFT.

UNIT-3:

Efficient Computation of the DFT: Fast Fourier Transform Algorithms: Direct Computation of the DFT, Radix-2 FFT Algorithms. **Implementation of Discrete Time Systems**: Structures for the Realization of Discrete Time Systems, **Structures for FIR Systems**: Direct Form Structure, Cascade Form Structures, Frequency Sampling Structures. **Structures for IIR Systems**: Discrete Form Structures, Signal Flow Graphs and Transposed Structures, Cascade Form Structures, Parallel Form Structures.

UNIT-4:

Design of Digital Filters: General Considerations: Causality and Its Implications, Characteristics of Practical Frequency Selective Filters. **Design of FIR Filters:** Symmetric and Antisymmetric FIR Filters, Design of Linear Phase FIR Filters Using Windows, Design of Linear Phase FIR Filters by the Frequency Sampling Method. **Design of IIR Filters From Analog Filters**: IIR Filter Design by Approximation of Derivatives, IIR Filter Design by Impulse Invariance, IIR Filter Design by the Bilinear Transformation. **Frequency Transformations:** Frequency Transformations in the Analog Domain, Frequency Transformations in the Digital Domain.

UNIT-5:

Introduction to programmable DSPs: Multiplier and Multiplier Accumulator, Modified bus structures and memory access schemes in P-DSPs, Multiple Access Memory, Multi ported memory, VLIW architecture, Pipelining, Special addressing modes, On-Chip Peripherals. **Architecture of TMS320C5X**: Introduction, Bus Structure, Central Arithmetic Logic Unit, Auxiliary Register ALU, Index Register, Auxiliary Register Compare Register, Block Move Address Register, Block Repeat Registers, Parallel Logic Unit, Memory mapped registers, program controller, some flags in the status registers, On- chip memory, On-chip peripherals.TMS320C5X Assembly Language Instructions.

Reference Books:

1. Discrete Time Signal Processing – A.V.Oppenheim and R.W. Schaffer, 3rd Edition, Pearson, 2014.
2. Digital Signal Processing-P. Ramesh Babu, 5th Edition, SCITECH Publishers.

TEXT BOOKS:

1. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, DimitrisG. Manolakis, 4th Edition, Pearson Education, 2007.
2. Digital Signal Processors – Architecture, Programming and Applications,, B.Venkataramani, M.Bhaskar, TATA McGraw Hill, 2002.

e- Resources: -

- https://nptel.ac.in/courses/117/101/117101093
- https://www.geeksforgeeks.org/digital-signal-processing-dsp/
- https://www.pdfdrive.com/digital-signal-processing-principles-algorithms-and-applications-e184102290.html

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III Year II Semester	ANALOG IC DESIGN (BT24EC32P2A)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the concepts of MOS Devices and Modeling.
- Design and analyze any Analog Circuits in real time applications.
- Extend the Analog Circuit Design to Different Applications in Real Time.
- Analyze and design CMOS amplifiers, comparators, oscillators, and PLL-based analog circuits.
- Evaluate the performance of analog ICs in terms of gain, bandwidth, noise, power, and stability.
- Understand of Open-Loop Comparators and Different Types of Oscillators.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	-	-	-	-	-	-	-	-	3	2
C02	3	3	3	2	2	2	2	-	-	-	-	-	3	3
CO3	2	3	3	2	2	2	2	-	-	-	-	-	3	3
CO4	3	3	3	2	2	2	2	-	-	-	-	-	3	3
CO5	3	2	2	3	2	2	2	-	-	-	-	-	3	3
CO6	2	2	2	2	2	-	-	-	-	-	-	-	2	2

UNIT -I:

MOS Devices and Modelling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modelling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III: CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures. CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -IV:

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete- Time Comparators.

UNIT -V:

Oscillators & Phase-Locked Loops: General Considerations, Ring Oscillators, LC Oscillators, Voltage Controlled Oscillators. Simple PLL, Charge Pump PLLs, Non-Ideal Effects in PLLs, Delay Locked Loops, Applications.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, Second Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition,2010.

REFERENCES:

1. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition,2010.
2. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn,2013.

e- Resources: -

- https://nptel.ac.in/courses/108/106/108106106
- https://www.ece.uc.edu/~omearac/AnalogCMOS/
- https://www.pdfdrive.com/cmos-analog-circuit-design-d158909440.html

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III Year II Semester	SATELLITE COMMUNICATION (BT24EC32P2B)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the concepts, applications and subsystems of Satellite communications.
- Derive the expression for G/T ratio and to solve some analytical problems on satellite link design.
- Understand the various types of multiple access techniques and architecture of earth station design.
- Analyze satellite link performance and multiple access techniques for practical satellite communication systems.
- Evaluate the impact of orbital parameters, subsystem characteristics, and propagation effects on satellite communication system performance.
- Understand the concepts of GPS and its architecture.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	1	-	-	-	-	-	-	-	-	1	1	1
CO2	3	3	2	3	2	-	-	-	-	-	-	1	2	3
CO3	3	2	3	2	1	-	-	-	-	-	-	1	1	2
CO4	3	3	3	3	2	-	-	-	-	-	-	2	2	2
CO5	3	3	2	3	1	-	1	-	-	-	-	2	1	1
CO6	2	2	3	2	2	1	-	-	-	-	-	2	3	2

UNIT I INTRODUCTION: Origin of Satellite Communications, Historical Back-ground, Basic Concepts of Satellite Communications, Frequency allocations for Satellite Services, Applications, Future Trends of Satellite Communications.
ORBITAL MECHANICS AND LAUNCHERS: Orbital Mechanics, Look Angle determination, Orbital perturbations, Orbit determination, launches and launch vehicles, Orbital effects in communication systems performance.

UNIT II SATELLITE SUBSYSTEMS: Attitude and orbit control system, telemetry, tracking, Command and monitoring system, power systems, communication subsystems, Satellite antennas, Equipment reliability and Space qualification.

UNIT III SATELLITE LINK DESIGN: Basic transmission theory, link equation, C/N ratio, system noise temperature and G/T ratio, Design of down links, up link design, Design of satellite links for specified C/N, System design example.

UNIT IV MULTIPLE ACCESS: Frequency division multiple access (FDMA): Intermodulation, Calculation of C/N. Time division Multiple Access (TDMA); Frame structure, Examples. Code Division Multiple access (CDMA): Spread spectrum transmission and reception.
EARTH STATION TECHNOLOGY: Introduction, basic architecture, Transmitters, Receivers, Antennas, Tracking systems, Terrestrial interface, Primary power test methods.

UNIT V LOW EARTH ORBIT AND GEO-STATIONARY SATELLITE SYSTEMS: Orbit consideration, coverage and frequency considerations, Delay & Throughput considerations, System considerations, Operational NGSO constellation Designs.
GLOBAL NAVIGATION SATELLITE SYSTEM(GNSS):
Introduction, various GNSS: GPS, GLONASS, GALILEO, BeiDou, QZSS, IRNSS. GPS-location principle, GPS navigation message, GPS receiver operation, differential GPS; IRNSS-introduction, IRNSS satellites, IRNSS constellation, IRNSS configuration, IRNSS services, navigation data, applications of IRNSS; multi GNSS.

TEXT BOOKS:
1. Satellite Communications – Timothy Pratt, Charles Bostian and Jeremy Allnutt, WSE, Wiley Publications, 3RD Edition, 2020.
2. Satellite Communications Engineering – Wilbur L. Pritchard, Robert A Nelson and Henri G. Suyderhoud, 2nd Edition, Pearson Publications, 2003.

REFERENCES:
1. Satellite Communications: Design Principles – M. Richharia, BS Publications, 2nd Edition, 2003.
2. Satellite Communication - D.C Agarwal, Khanna Publications, 5th Ed.
3. Fundamentals of Satellite Communications – K.N. Raja Rao, PHI, 2004
4. Satellite Communications – Dennis Roddy, McGraw Hill, 2nd Edition, 1996.

e- Resources: -

- https://nptel.ac.in/courses/117/105/117105107
- https://www.scribd.com/document/384182476/Satellite-Communications-Pratt
- https://www.pdfdrive.com/satellite-communications-d155108317.html

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III Year II Semester	SMART AND WIRELESS INSTRUMENTATION (BT24EC32P2C)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Analyze Smart and Wireless Instrumentation with respect to various performance parameters.
- Design and develop Applications using WSN (Wireless sensor Network).
- Demonstration of various Node architectures.
- Analyze wireless digital communication techniques such as source coding, channel coding, modulation, and error control used in WSNs.
- Demonstration of Fundamentals of wireless digital communication.
- Analyze the power sources, Demonstrate an ability to design strategies as per needs and specifications.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	2	-	-	-	-	-	-	1	2	2
CO2	3	3	3	2	3	1	2	-	2	-	1	2	3	3
CO3	3	2	3	1	2	-	-	-	-	-	-	1	2	3
CO4	3	3	2	3	2	-	-	-	-	-	-	2	2	1
CO5	3	2	1	1	1	-	-	-	-	-	-	1	1	1
CO6	2	3	3	2	2	-	3	-	-	-	-	2	2	2

UNIT – 1: Introduction:
Smart Instrumentation (Materials, automation systems, ensign and Sensors, Sensor Classifications, Wireless Sensor Networks, History of Wireless Sensor networks (WSN), Communication in a WSN, important design constraints of a WSN like Energy, Self-Management, Wireless Networking, Decentralized Management, Design Constraints, Security etc.

UNIT – 2: Node architecture: The sensing subsystem, Analog to Digital converter, the processor subsystem, architectural overview, microcontroller, digital signal processor, application specific integrated circuit, field programmable gate array (FPGA), comparison, communication interfaces, serial peripheral interface, inter integrated circuit, the IMote node architecture, The XYZ node architecture, the Hog throb node architecture.

UNIT – 3: Fundamentals of Wireless Digital Communication: Basic components, source encoding, the efficiency of a source encoder, pulse code modulation and delta modulation, channel encoding, types of channels, information transmission over a channel, error recognition and correction, modulation, modulation types, quadratic amplitude modulation, signal propagation.

UNIT – 4: Frequency of Wireless Communication: Development of Wireless Sensor Network based on Microcontroller and communication device-Zigbee Communication device. Power

sources- Energy Harvesting Solar and Lead acid batteries-RF Energy /Harvesting-Energy Harvesting from vibration Thermal Energy Harvesting-Energy Management Techniques Calculation for Battery Selection.

UNIT – 5: Applications:
Structural health monitoring - sensing seismic events, single damage detection using natural frequencies, multiple damage detection using natural frequencies, multiple damage detection using mode shapes, coherence, piezoelectric effect, traffic control, health care - available sensors, pipeline monitoring, precision agriculture, active volcano, underground mining.

Text Books:

1. Fundamentals of wireless sensor networks: theory and practice - WaltenegusDargie, Christian Poellabauer, A John Wiley and Sons, Ltd., Publication.
2. Smart Sensors, Measurement and Instrumentation, Subhas Chandra Mukhopadhyay, Springer Heidelberg, New York, Dordrecht London, 2013.
3. Wireless Sensors and Instruments: Networks, Design and Applications, HalitEren, CRC Press, Taylor and Francis Group, 2006.

Reference Books:

1. UvaisQidwai, Smart Instrumentation: A data flow approach to Interfacing", Chapman & Hall; 1st Edn, December 2013.
2. Wireless Sensor Networks: Architectures and Protocols, Edgar H. Callaway Jr. and Ed gar H. Callaway.

e- Resources: -

- https://nptel.ac.in/courses/108/106/108106118
- https://www.ti.com/technologies/zigbee/overview.html
- https://www.mdpi.com/journal/sensors/special_issues/WSN
- https://www.sciencedirect.com/topics/computer-science/wireless-sensor-network

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III Year II Semester	MACHINE LEARNING (BT24EC32P2D)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Define machine learning and its different types and understand their applications.
- Explain the various techniques involved in pre-processing of data for Data Analysis.
- Apply various supervised learning algorithms including decision trees and k-nearest neighbours (k-NN) etc.
- Apply supervised machine learning algorithms for classification and regression tasks.
- Implement unsupervised learning techniques, viz., K-means clustering etc.
- Learn about various performance metrics and explore them in various applications of implementing Machine learning Algorithms.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	-	-	1	-	-	-	-	-	-	1	1	1
CO2	2	3	2	3	3	-	-	-	-	-	-	1	2	2
CO3	3	3	3	3	3	1	-	-	1	-	-	2	3	3
CO4	3	3	3	3	3	-	-	-	-	-	-	2	3	3
CO5	2	2	3	3	3	-	-	-	-	-	-	2	2	3
CO6	2	3	2	3	3	-	-	-	1	1	-	2	2	3

UNIT-I: Introduction to Machine Learning:

What is Machine Learning?, Traditional programming approach vs Machine learning approach, History and Evolution of Machine Learning, Learning by Rote vs Learning by Induction, **Paradigms for ML** - Supervised ML, Unsupervised ML, Reinforcement ML, **Datatypes in ML** - Quantitative data (Continuous, Discrete), Qualitative data (Structured, Semi structured, Unstructured), Nominal data, Ordinal data, Interval data, Ratio data, Stages involved in Machine Learning, Main challenges of ML, Applications of Machine Learning, **IDE's for ML Programming** - Jupyter Notebook, Spyder, PyCharm, Google Colab, R Studio, VS Code, **Basic packages to deal with ML** - Numpy, Scipy, Pandas, Scikit-learn, Matplotlib, Seaborn, **Programming Languages for Machine Learning** - Python, Java, R, JavaScript, C++

UNIT - II: Explorative Data Analysis (EDA):

What is EDA? Why EDA is important?, **Types of EDA** - Univariate Analysis, Bivariate Analysis, Multivariate Analysis, **Data Cleaning** - Data Acquisition, Analyzing the data Dealing with duplicate data, Dealing with missing values, Dealing with outliers **Scaling and Transformations** - Feature Scaling and Transformation, Univariate nonlinear Transformations, **Dimensionality Reduction** - Principal Component Analysis (PCA), **Feature Engineering** - Handling Categorical attributes (One-Hot-Encoding), **Feature Expansion** - Interactions and Polynomials, **Automatic Feature Selection** - Univariate Statistics, Model-Based Feature Selection, Iterative Feature Selection

UNIT-III: Supervised Machine Learning:

What is Supervised Machine Learning?, General architecture of Supervised ML, **Types of Supervised ML** - Classification and Regression, **Different Classification Algorithms** - K-Nearest Neighbor (KNN) Classifier, Linear Models, Logistic Regression, Naive Bayes Classifiers, Decision Tree Classifier, **Ensemble learning and Decision Trees** - Voting, Bagging and pasting, Random Forests, AdaBoost, Gradient Boosting, Stacking, Support Vector Classifier (SVC)Neural Networks, **Different Regression Algorithms** - K-Neighbors Regressor, Linear Regression, Ridge Regression, Lasso Regression, Polynomial Regression, Support Vector Regressor (SVR), Decision Tree Regressor, Random Forest Regressor

UNIT-IV: Unsupervised Machine Learning –

What is Unsupervised Machine Learning?, General architecture of Unsupervised Machine Learning, Challenges in Unsupervised ML, **Clustering** - Introduction to Clustering, Soft clustering vs Hard Clustering, K-Means Clustering algorithm, Centroid-based clustering algorithm, Divisive Clustering and Agglomerative Clustering, DBSCAN

UNIT V- Model Evaluation metrics, Fine tuning the model and Visualizations -

Evaluation Metrics for Classification - Confusion Matrices, Accuracy, Precision, Recall, F1-Score, Precision-recall curves, ROC (Receiver Operating Characteristics) curves, Confusion Matrix, **Evaluation Metrics for Regression** - R^2, Mean Squared Error (MSE), Mean Absolute Error (MAE), Root Mean Squared Error (RMSE), **Evaluation Metrics for clustering** - Adjusted Random Index (ARI), Normalized Mutual Information (NMI), **Cross Validation** - Cross- Validation in scikit-learn, benefits of cross-validation, stratified k-fold cross validation, **Grid Search**- Simple Grid search, Grid search with cross validation, Randomized search, **Visualization**
- Univariate Analysis (Bar plot, Box plot, Count plot, Density plot, Histogram, Pieplot), Bivariate Analysis (Pair plot, Scatter plot, Bar plot, Stacked barplot, Multivariate Analysis (Heat Maps)

Text Books:

1. "Introduction to Machine Learning with Python", Andreas C.Muller&Sarah Guido, O'Reilly Publications.
2. "Hands-on Machine Learning with Scikit-Learn, Keras& TensorFlow", Aurelien Geron, O'Reilly Publications.
3. "Machine Learning Theory and Practice", M N Murthy, V S Ananthanarayana, Universities Press (India), 2024.

Reference Books:

1. "Machine Learning", Tom M. Mitchell, McGraw-Hill Publication, 2017.
2. "Machine Learning in Action",Peter Harrington, DreamTech
3. "Introduction to Data Mining", Pang-Ning Tan, Michel Stenbach, Vipin Kumar, 7th Edition, 2019.

e- Resources: -

- https://nptel.ac.in/courses/106/106/106106145
- https://towardsdatascience.com/exploratory-data-analysis-in-python-c9a77dfa39ce
- https://www.geeksforgeeks.org/k-means-clustering-introduction/

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III Year II Semester	BIO-MEDICAL INSTRUMENTATION (BT24EC32P3A)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Demonstrate a foundational understanding of the anatomy and physiology of the human body.
- Apply knowledge of different techniques used for measuring various physiological parameters.
- Explain modern imaging techniques employed in medical diagnosis and identify the diverse therapeutic equipment utilized in the biomedical field.
- Analyze patient monitoring systems and respiratory measurement instruments used in intensive care units.
- Understand and apply bio-telemetry principles for transmitting bioelectrical variables.
- Analyze patient safety measures and evaluate recent advancements in the medical field.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	-	-	-	1	-	-	-	-	-	1	2	-
CO2	3	3	3	2	2	2	-	-	-	-	-	1	3	2
CO3	3	2	2	3	2	2	1	-	-	-	-	2	3	2
CO4	2	3	3	2	2	3	-	-	1	-	-	1	3	2
CO5	3	2	3	2	3	1	-	-	-	-	-	2	3	3
CO6	2	2	1	2	1	3	-	3	-	-	-	2	2	1

UNIT – 1: Introduction: Factors to be considered in the design of medical instrumentation systems, Basic objectives of medical instrumentation system, Physiological systems of human body, Sources of Bioelectric potentials: Resisting and Action Potentials, Propagation of Action Potentials, The Bioelectric Potentials. Electrodes: Electrode theory, Bio Potential Electrodes, Biochemical Transducers, Introduction to bio-medical signals.

UNIT – 2: The Cardiovascular System: The Heart and Cardiovascular System, The Heart, Blood Pressure, Characteristics of Blood Flow, Heart Sounds, Cardio Vascular Measurements, Electrocardiography, Measurement of Blood Pressure, Measurement of Blood Flow and Cardiac output, Plethysmo graphy, Measurement of Heart Sounds, Event detection, PQRS & T-Waves inECG, the first & second Heart beats, ECG rhythm analysis, the di-crotic notch in the carotid pulse detection of events and waves, analysis of exercise ECG, analysis of event related potentials, correlation analysis of EEG channels, correlation of muscular contraction.

UNIT – 3: Patient Care & Monitory and Measurements in Respiratory System: The elements of Intensive Care Monitory, Diagnosis, Calibration and reparability of Patient Monitoring equipment, other instrumentation for monitoring patients, pace makers, defibrillators, the physiology of respiratory system, tests and instrumentation for mechanics of breathing, respiratory theory equipment, analysis of respiration.

UNIT – 4: Bio telemetry and Instrumentation for the Clinical Laboratory, Introduction to bio telemetry, Physiological parameters adaptable to bio telemetry, the components of bio telemetry system, implantable units, applications of telemetry in patient care – The blood, tests on blood cells, chemical test.

UNIT – 5: X-ray and radioisotope instrumentation and electrical safety of medical equipment: Generation of Ionizing radiation, instrumentation for diagnostic X-rays, special techniques, instrumentation for the medical use of radioisotopes, radiation therapy - Physiological effects of electrical current, shock Hazards from electrical equipment, Methods of accident prevention, Modern Imaging Systems: Tomography, Magnetic Resonance Imaging System, Ultrasonic Imaging System, Medical Thermography.

Text Books:

1. Biomedical Instrumentation and Measurements C.Cromwell, F.J.Weibell, E.A.Pfeiffer – Pearson education.
2. Biomedical Signal Analysis – Rangaraj, M. Rangayya – Wiley Inter Science – JohnWilley & Sons Inc.

Reference Books:

1. Hand Book of Bio-Medical Instrumentation – R.S. Khandpur, TMH.
2. Introduction to Bio-Medical Engineering – Domach, Pearson.
3. Introduction to Bio-Medical Equipment Technology – Cart, Pearson.

e- Resources: -

- https://nptel.ac.in/courses/108/106/108106148
- https://radiopaedia.org/articles/overview-of-medical-imaging
- https://nptel.ac.in/courses/108/105/108105081

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III Year II Semester	MICROWAVE ENGINEERING (BT24EC32P3B)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Able to apply Maxwell's equations and analyze wave propagation in Rectangular Wave Guide.
- Able to apply Maxwell's equations and analyze wave propagation in Cylindrical wave guide.
- Able to illustrate the Microwave O- Type tubes.
- Able to illustrate the HELIX TWTS and M-Type Tubes.
- Able to analyze Scattering parameters and characterize various microwave devices.
- Able to explain theory and analyze various Microwave active devices and measure various Microwave parameters (VSWR, Impedance, etc.).

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3	-	-	-	-	-	-	-	-	-	-	3	-
CO2	2	3	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	2	1	-	-	-	-	-	-	-	-	-	3	-
CO4	3	1	-	1	-	-	-	-	-	-	-	-	3	-
CO5	3	2	1	-	-	-	-	-	-	-	-	-	3	-
CO6	3	2	-	-	-	-	-	-	-	-	-	-	3	-

UNIT-I

MICROWAVE TRANSMISSION LINES: Introduction, Microwave Spectrum and Bands, Applications of Microwaves. Rectangular Waveguides – TE/TM mode analysis, Expressions for Fields, Characteristic Equation and Cut-off Frequencies, Filter Characteristics, Dominant and Degenerate Modes, Sketches of TE and TM mode fields in the cross-section, Mode Characteristics – Phase and Group Velocities, Wavelengths and Impedance Relations; Power Transmission and Power Losses in Rectangular Guide. Related Problems. MICROSTRIP LINES– Introduction, Zo Relations, Effective Dielectric Constant, Losses, Q factor.

UNIT II

MICROWAVE TUBES: Limitations and Losses of conventional tubes at microwave frequencies. Microwave tubes – O type and M type classifications. O-type tubes : 2 Cavity Klystrons – Structure, Reentrant Cavities, Velocity Modulation Process and Applegate Diagram, Bunching Process and Small Signal Theory – Expressions for o/p Power and Efficiency. Reflex Klystrons – Structure, Applegate Diagram and Principle of working, Mathematical Theory of Bunching, Power Output,

Efficiency, Electronic Admittance; Oscillating Modes and o/p Characteristics, Electronic and Mechanical Tuning. Applications.

UNIT-III

HELIX TWTS: Significance, Types and Characteristics of Slow Wave Structures; Structure of TWT and Amplification Process (qualitative treatment), Suppression of Oscillations, Nature of the four Propagation Constants, Gain Considerations(qualitative treatment).**M-type Tubes** Introduction, Cross-field effects, Magnetrons – Different Types, 8-Cavity Cylindrical Travelling Wave Magnetron – Hull Cut-off and Hartree Conditions, Modes of Resonance and PI-Mode Operation, Separation of PI-Mode, o/p characteristics.

UNIT-IV

WAVEGUIDE COMPONENTS AND APPLICATIONS: Coupling Mechanisms – Probe, Loop, Aperture types. Waveguide Discontinuities – Waveguide irises, Tuning Screws and Posts, Matched Loads. Waveguide Attenuators – Resistive Card, Rotary Vane types; Waveguide Phase Shifters – Dielectric, Rotary Vane types, Scattering Matrix– Significance, Formulation and Properties, S-Matrix Calculations for – 2,3,4 port Junctions: E-plane and H-plane Tees, Magic Tee, Hybrid Ring; Directional Couplers – 2Hole, Bethe Hole types, S-Matrix Calculations Ferrite Components– Faraday Rotation, Gyrator, Isolator, Circulator, Related Problems.

UNIT-V

MICROWAVE SOLID STATE DEVICES: Introduction, Classification, Applications. TEDs – Introduction, Gunn Diode – Principle, RWH Theory, Characteristics, Basic Modes of Operation, Oscillation Modes.

MICROWAVE MEASUREMENTS: Description of Microwave Bench – Different Blocks and their Features, Precautions; Microwave Power Measurement – Bolometer Method. Measurement of Attenuation, Frequency, Q- factor, Phase shift, VSWR, Impedance Measurement.

TEXT BOOKS:

1. Foundations for Microwave Engineering – R.E. Collin, IEEE Press, John Wiley, 2nd Edition, 2002.
2. Microwave Engineering- Annapurna Das and Sisir K.Das, Mc Graw Hill Education, 3rd Edition.

REFERENCES:

1. Microwave Devices and Circuits – Samuel Y. Liao, PHI, 3rd Edition,1994.
2. Microwave Engineering – G S N Raju , I K International.
3. Microwave and Radar Engineering-M.Kulkarni, Umesh Publications, 3rd Edition.

e- Resources: -

- https://nptel.ac.in/courses/108/105/108105081

- https://www.electronics-tutorials.ws/amplifier/magnetron.html
- https://www.ti.com/lit/an/slyy123/slyy123.pdf

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III Year II Semester	EMBEDDED SYSTEMS (BT24EC32P3C)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Know basics of embedded system, classification, memories, different communication interface and what embedded firmware is and its role in embedded system, different system components.
- Distinguish all communication devices in embedded system, other peripheral device.
- Design embedded firmware using interrupts, device drivers, and DMA for efficient real-time system operation.
- Analyze and select appropriate RTOS features and scheduling strategies for real-time embedded applications.
- DistinguishconceptsofCversusembeddedCandcompilerversuscross-compiler.
- Choose an operating system, and learn how to choose an RTOS.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	1	2	-	-	-	-	-	-	1	2	2
CO2	3	3	2	2	2	-	-	-	-	-	-	1	2	2
CO3	3	3	3	2	3	-	-	-	1	-	-	2	3	3
CO4	3	3	3	3	2	-	-	-	-	-	-	2	3	2
CO5	3	2	2	2	3	-	-	-	-	-	-	1	1	3
CO6	2	3	3	2	2	-	-	-	-	-	-	2	2	2

Unit-I:

Introduction: Embedded System-Definition, History, Classification, application areas and purpose of embedded systems, The typical embedded system-Core of the embedded system, Memory, Sensors and Actuators, Communication Interface, Embedded firmware, PCB and passive components. Characteristics, Quality attributes of an Embedded systems, Application-specific and Domain-Specific examples of an embedded system, Main processing elements of embedded system, hardware and software partitions.

Unit-II:

Embedded Hardware Design: Analog and digital electronic components, I/O types and examples, Serial communication devices, Parallel device ports, Wireless devices, Timer and counting devices, Watch dog timer, Real time clock.

Unit-III:

Embedded Firmware Design: Embedded Firmware design approaches, Embedded Firmware development languages, ISR concept, Interrupt sources, Interrupt servicing mechanism, Multiple interrupts, DMA, Device driver programming, Concepts of C versus Embedded C and Compiler versus Cross-compiler.

Unit-IV:

Real Time Operating System: Operating system basics, Types of operating systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Threads, Processes and Scheduling, Task Scheduling, Communication, Synchronization, Device Drivers, How to choose an RTOS. Electronics and Communication Engineering.

Hardware Software Co-Design: Fundamental Issues in Hardware Software Co-Design, Computational models in embedded design, Hardware software Trade-offs, Integration of Hard ware and Firm ware, ICE.

Unit-V:

Embedded System Development: The integrated development environment, Types of files generated on cross-compilation, Dissembler/De-compiler, Simulators, Emulators and Debugging, Target hardware debugging, Boundary Scan, Embedded Software development process and tools.

Embedded System Implementation and Testing: The main software utility tool, CAD and the hardware, Translation tools-Pre-processors, Interpreters, Compilers and Linkers, Debugging tools, Quality assurance and testing of the design, Testing on hostmachine, Simulators, Laboratory Tools. Test and evolution of an embedded system (Build in selftest etc).

Case study-typical embedded system design flow with an example.

Text Books:

1. Embedded Systems Architecture By Tammy Noergaard, Elsevier Publications,2005.
2. Embedded System Design, Frank Vahid,Tony Givargis, John Wiley Publications.

References:

1. Embedding system building blocks By Labrosse, CMP publishers.

e- Resources: -

- https://nptel.ac.in/courses/108/108/108108103
- https://www.ti.com/embedded/overview.html
- https://www.arm.com/why-arm/embedded-tools

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III Year II Semester	ARTIFICIAL INTELLIGENCE (BT24EC32P3D)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the concepts of computational intelligence like machine learning.
- Ability to get the skill to apply machine learning techniques to address the real time Problems in different areas.
- Understand the Neural Networks and its usage in machine learning application.
- Apply probabilistic and non-monotonic reasoning techniques to handle uncertainty in intelligent systems.
- Apply principles and algorithms evaluate models generated from data.
- Apply the algorithms to a real-world problems.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	-	1	-	-	-	-	-	-	1	1	2
CO2	3	3	3	2	3	1	-	-	1	-	-	2	2	3
CO3	3	3	2	2	2	-	-	-	-	-	-	2	3	2
CO4	3	3	2	3	1	-	-	-	-	-	-	1	2	1
CO5	2	3	2	3	3	-	-	-	-	-	-	2	1	2
CO6	3	3	3	2	3	2	1	-	2	1	1	3	3	3

UNIT-1

What is AI (Artificial Intelligence)? : The AI Problems, The Underlying Assumption, What are AI Techniques, The Level Of The Model, Criteria For Success, Some General References, One Final Word Problems, State Space Search & Heuristic Search Techniques: Defining The Problems As A State Space Search, Production Systems, Production Characteristics, Production System, Characteristics And Issues In The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-First Search, Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

UNIT-2

Knowledge Representation Issues: Representations And Mappings, Approaches to Knowledge Representation. Using Predicate Logic: Representation Simple Facts in Logic, Representing Instance and Isa Relationships, Computable Functions and Predicates, Resolution. Representing Knowledge Using Rules: Procedural Versus Declarative Knowledge, Logic Programming, Forward Versus Backward Reasoning.

UNIT-3

Symbolic Reasoning Under Uncertainty: Introduction to No monotonic Reasoning, Logics for Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays' Theorem, Factors and Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory.

UNIT-4

Fuzzy Logic. Weak Slot-and-Filler Structures: Semantic Nets, Frames. Strong Slot-and-Filler Structures: Conceptual Dependency, Scripts, CYC.

UNIT-5

Game Playing: Overview, And Example Domain: Overview, Mini Max, Alpha-Beta Cut-off, Refinements, Iterative deepening, The Blocks World, Components Of A Planning System, Goal Stack Planning, Nonlinear Planning Using Constraint Posting, Hierarchical Planning, Reactive Systems, Other Planning Techniques. Understanding: What is understanding? What makes it hard? As constraint satisfaction.

Natural Language Processing: Introduction, Syntactic Processing, Semantic Analysis, Semantic Analysis, Discourse and Pragmatic Processing, Spell Checking Connectionist Models: Introduction: Hopfield Network, Learning In Neural Network, Application Of Neural Networks, Recurrent Networks, Distributed Representations, Connectionist AI And Symbolic AI.

Text Books:

1. Elaine Rich and Kevin Knight "Artificial Intelligence", 2nd Edition, Tata Mcgraw-Hill, 2005.
2. Stuart Russel and Peter Norvig, "Artificial Intelligence: A Modern Approach", 3rd Edition, Prentice Hall, 2009.

References:

1. **Artificial Intelligence: A Modern Approach** – Stuart Russell, Peter Norvig, 4th Edition, Pearson, 2021.
2. **Neural Networks and Deep Learning** – Charu Aggarwal, Springer, 2018.

e- Resources: -

- https://nptel.ac.in/courses/106/105/106105164
- https://www.ai-class.com/
- https://www.tutorialspoint.com/fuzzy_logic/index.htm

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III Year II Semester	LINEAR AND DIGITAL IC APPLICATIONS (BT24EC32O2A)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Analyze and design various configurations of operational amplifiers, and applications such as instrumentation amplifiers, voltage regulators, comparators, and waveform generators.
- Design and implement active filters and waveform generators using op-amps, IC-555, and IC-565, and evaluate their performance for signal processing applications.
- Compare different data conversion techniques (DAC and ADC) and implement digital-to-analog and analog-to-digital conversion circuits in real-time applications.
- Analyze and implement DAC and ADC circuits and evaluate their performance parameters for real-time applications.
- Apply combinational logic ICs such as multiplexers, de-multiplexers, encoders, decoders, and arithmetic circuits to solve complex digital design problems.
- Develop sequential circuits using flip-flops, counters, and shift registers, and analyze their use in digital memory systems, including ROM, RAM, and their variants.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	-	-	-	-	-	-	2	3	2
CO2	3	3	3	2	2	-	-	-	-	-	-	2	3	3
CO3	3	2	2	2	1	-	-	-	-	-	-	1	2	2
CO4	3	3	3	3	2	-	-	-	-	-	-	2	2	2
CO5	3	3	3	2	1	-	-	-	-	-	-	2	2	3
CO6	3	3	3	2	1	-	-	-	-	-	-	2	2	3

UNIT–I

Operational Amplifier: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, features of 741 Op-Amp, Modes of Operation-Inverting, Non-Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT-II

Op-Amp, IC-555 & IC565 Applications: Introduction to Active Filters, Characteristics of Bandpass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, Waveform Generators – Triangular, Sawtooth, Square Wave, IC555 Timer-Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL-Block Schematic, principle and Applications.

UNIT-III

Data Converters: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs – Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.

UNIT-IV

Combinational Logic ICs: Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoders, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, De-multiplexers, Priority Generators/Checkers, Parallel Binary Adder/Subtractor, Magnitude Comparators.

UNIT-V

Sequential Logic IC's and Memories: Familiarity with commonly available 74XX & CMOS40XX Series ICs - All Types of Flip-flops, Synchronous Counters, Decade Counters, Shift Registers. Memories - ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.

TEXTBOOKS:

1. Ramakanth A.Gayakwad-Op-Amps & LinearICs, PHI,2003.
2. FloydandJain-DigitalFundamentals,8th Ed.,Pearson Education,2005.

REFERENCE BOOKS:

1. D.Roy Chowdhury–Linear Integrated Circuits, New Age International(p) Ltd ,2nd Ed.,2003.
2. John.F.Wakerly–DigitalDesignPrinciplesandPractices,3rd Ed.,Pearson,,2009.
3. Salivahana-Linear Integrated Circuits and Applications, TMH, 2008.
4. William D.Stanley-Operational Amplifiers with Linear Integrated Circuits, 4th Ed.,Pearson Education India, 2009

e- Resources:-

- https://epgp.inflibnet.ac.in
- NPTEL Linear ICs, TI Op-Amp Handbook
- https://mrcet.com/downloads/digital_notes/EEE/13092021/LINEAR%20%26%20DIGITAL%20IC.pdf

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III Year II Semester	PRINCIPLES OF COMMUNICATIONS (BT24EC32O2B)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Analyze the performance of analog modulation schemes in time and frequency domains.
- Analyze the performance of angle modulated signals.
- Characterize analog signals in time domain as random processes and noise.
- Characterize the influence of channel on analog modulated signals.
- Determine the performance of analog communication systems in terms of SNR.
- Analyze pulse amplitude modulation, pulse position modulation, pulse code modulation and TDM systems.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	1	-	-	-	-	-	-	-	1	1
CO2	3	3	2	2	1	-	-	-	-	-	-	-	1	2
CO3	3	3	2	2	2	-	-	-	-	-	-	-	1	2
CO4	3	3	3	2	2	-	-	-	-	-	-	-	2	2
CO5	3	3	3	3	2	-	-	-	-	-	-	-	2	2
CO6	3	3	3	3	3	-	-	-	-	-	-	-	2	3

UNIT1: Basic tools for communication, Fourier Series/Transform, Properties, Autocorrelation, Energy Spectral Density, Parsevals Relation, Amplitude Modulation (AM), Spectrum of AM, Envelope Detection, Power Efficiency, Modulation Index.

UNIT2: Double Sideband Suppressed Carrier (DSB-SC) Modulation, Demodulation, Costas Receiver, Single Sideband Modulation (SSB), Hilbert Transform, Complex Pre-envelope/ Envelope, Demodulation of SSB, Vestigial Sideband Modulation (VSB).

UNIT 3: Angle Modulation, Frequency Modulation (FM), Phase Modulation (PM), Modulation Index, Instantaneous Frequency, Spectrum of FM Signals, Carsons Rule for FM Bandwidth, Narrowband FM Generation, Wideband FM Generation via Indirect Method, FM Demodulation.

UNIT 4: Introduction to Sampling, Spectrum of Sampled Signal, Aliasing, Nyquist Criterion, Signal Reconstruction from Sampled Signal, Pulse Amplitude Modulation, Quantization, Uniform Quantizers – Midrise and Midtread, Quantization noise, , Non uniform Quantizers, Delta Modulation, Differential Pulse Code Modulation (DPCM).

UNIT 5: Basics of Probability, Conditional Probability, MAP Principle, Random Variables, Probability Density Functions, Applications in Wireless Channels, Basics of Random Processes ,Gaussian Random Process, Noise.

TEXTBOOKS:

1. Simon Haykin, Communications Systems, 4th Edition. John Wiley and Sons, Inc.
2. Fundamentals of Wireless Communication by David Tse.

REFERENCE BOOKS:

1. Communication Systems – Simon Haykin, 4th Edition, John Wiley & Sons, Inc.
2. Modern Digital and Analog Communication Systems – B.P. Lathi, 4th Edition, Oxford University Press, 2010.

e- Resources:-

- https://nptel.ac.in/courses/117/101/117101024/
- https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-450-principles-of-digital-communication-spring-2006/

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III Year II Semester	PRINCIPLES OF SIGNAL PROCESSING (BT24EC32O2C)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Acquire the knowledge in signals and systems.
- Get familiarized with various transforms to analyze continuous time signals.
- Understand sampling theorem and z-transform.
- Apply sampling theorem and Z-transform techniques to analyze and process discrete-time signals.
- Get familiarized with the transforms of discrete time signals.
- Design the digital filter design

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	1	1	-	-	-	-	-	-	-	1	1
CO2	3	3	2	2	2	-	-	-	-	-	-	-	1	2
CO3	3	3	2	2	2	-	-	-	-	-	-	-	1	2
CO4	3	3	3	2	2	-	-	-	-	-	-	-	2	2
CO5	3	3	3	2	2	-	-	-	-	-	-	-	2	3
CO6	3	3	3	3	3	-	-	-	-	-	-	-	2	3

Unit- I: Introduction:

Definition of Signals and Systems, Classification of Signals, Classification of Systems, Operations on signals: time-shifting, time-scaling, amplitude-shifting, Amplitude - scaling. Problems on classification and characteristics of Signals and Systems. Complex exponential and sinusoidal signals, impulse Function, step function, signum function and ramp function. Introduction, Linear system, impulse response, Linear time invariant (LTI) system, Linear time invariant(LTV) system, Concept of convolution in time domain and frequency domain, Graphical representation of convolution, Transfer function of a LTI system, Related problems.

Unit-II: Analysis of continuous time signals

Fourier Series and Fourier Transform:

Fourier series representation of continuous time periodic signals, Dirichlet's conditions, Trigonometric Fourier series and Exponential Fourier series,. Deriving Fourier transform from Fourier series, Fourier transform of standard signals, properties of Fourier transforms, Related problems.

Laplace Transforms:

Introduction, Concept of region of convergence (ROC) for Laplace transforms, Properties of L.T's, Inverse Laplace transform, Relation between Laplace Transform and Fourier Transform of a signal.

Unit III: **Sampling Theorem**: Graphical and analytical proof or Band Limited Signals, impulse sampling, Reconstruction of signal from its samples, Aliasing.
Z–Transforms: Concept of Z-Transform of a discrete sequence. Region of convergence in Z-Transform, Inverse Z-transform, properties of Z-transforms.

Unit IV: Fourier Transforms of discrete signal: Fourier Transform of Discrete Signal, Properties, and Inverse Fourier Transforms, related problems.
Discrete Fourier Transforms: Definition, Properties, Inverse DFT, related problems.
Fast Fourier Transform: Decimation in Time domain and Decimation in Frequency Algorithms.

Unit V: Digital Filters: **Structures of IIR filters and FIR filters**: Director form–1 and Direct form 2; cascade form; parallel form **Analog filter design** LPF, BPF, HPF and BEF filter design using Butterworth **Frequency Transformations:** Analog to Analog; Digital and Digital **IIR Filter Design:** IIR filter from analog filter – IIR filter design by Impulse Invariance, Bilinear transformation. **FIR Filter Design:** Filter design using windowing techniques. Rectangular Window, Hamming Window, Hanning Window.

Text Books:

1. Signals, Systems & Communications - B. P. Lathi, BS Publications, 2003.
2. Digital Signal Processing - P. Ramesh Babu, 5th Edition, SCITECH Publishers.

Reference Books:

1. Signals & Systems – Simon Haykin and VanVeen, Wiley, 2nd Edition, 2007.
2. Signals and Systems-A.V. Oppenheim, A.S. Willsky and S.H. Nawab, PHI, 2ndEdn, 1997.
3. Discrete Time Signal Processing – A.V.Oppenheim and R.W. Schaffer, 3rd Edition, Pearson, 2014.

e- Resources:-

- https://nptel.ac.in/courses/108/105/108105077/
- https://www.geeksforgeeks.org/fast-fourier-transform-introduction/

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III Year II Semester	MICROPROCESSORS & MICROCONTROLLERS (BT24EC32O2D)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand the architecture of 8086 microprocessor and their modes of operation.
- Demonstrate various addressing modes and assembly language programming for 8086 microprocessors.
- Analyze interfacing of 8086 microprocessors with different Peripherals.
- To design and develop the new interface ideas in real time applications.
- Demonstrating the architecture of 8051 Microcontrollers, its instruction set and interfacing with different peripherals.
- Understand the features and instruction set of ARM Processor.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	-	-	-	-	-	1
CO2	2	2	-	-	-	-	-	-	-	-	-	-	-	1
CO3	2	2	2	-	-	-	-	-	-	-	-	-	-	2
CO4	2	2	2	-	-	-	-	-	-	-	-	-	-	2
CO5	2	1	-	-	-	-	-	-	-	-	-	-	-	2
CO6	2	2	2	-	-	-	-	-	-	-	-	-	-	2

UNIT-1:

Introduction: Microprocessor based system, Origin of microprocessors, Harvard and Von Neumann architectures with examples, Microprocessor Unit versus Microcontroller Unit.

8086 Architecture: internal architecture of 8086 microprocessor, register organization, physical memory organization, general bus operation.

UNIT-2:

8086 Programming: instruction set, addressing modes, assembler directives, programming with assembler, writing simple programs with an assembler, stack and stack structure, interrupts and interrupt service routines, interrupt cycle of 8086.

UNIT-3:

8086 Interfacing: Semiconductor memories interfacing (RAM, ROM), Intel 8255 programmable peripheral interface, Interfacing switches and LEDS, Interfacing seven segment displays, Intel 8251 USART architecture and interfacing, stepper motor, A/D and D/A converters.

UNIT-4:

Intel 8051 MICROCONTROLLER and Interfacing

Introduction to microcontrollers, internal architecture of 8051 microcontroller, I/O ports and memory organization, MCS51 addressing modes and instruction set, assembly language programming, simple programs, counters/timers, serial data input/output, interrupts. Interfacing to 8051: A/D and D/A Convertors, keyboard, LCD Interfacing.

UNIT-5:

ARM Architectures and Processors: introduction to CISC and RISC architectures, ARM Architecture, ARM Processors Families, Introduction to 16/32 bit processors, ARM7 architecture and organization, Thumb instructions, ARM Cortex-M3 Processor Functional Description.

TEXTBOOKS:

1. Advanced microprocessors and peripherals by K. M. Bhurchandi, A. K. Ray 3e
2. The 8051 Microcontrollers and Embedded systems Using Assembly and C, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D.McKinlay; Pearson 2-Edition,2011.
3. Microprocessors and Microcontrollers by N. Senthil Kumar, M. Saravanan and S. Jeevanathan Oxford higher education

REFERENCE BOOKS:

1. Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers: A Practical Approach in English, by Dr. Alexander G. Dean, Published by Arm EducationMedia,2017.
2. Cortex-M3TechnicalReference Manual.
3. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu., Newnes Third edition

e- Resources: -

- https://nptel.ac.in/courses/108/108/108108117
- https://www.electronics-tutorials.ws/microcontroller/8051.html
- https://www.keil.com/cortex-m3/

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III Year II Semester	VLSI DESIGN LAB (BT24EC3204)	L	T	P	C
		0	0	3	1.5

Laboratory Objective

The objective of this laboratory course is to enable students to design, simulate, and implement CMOS-based digital and analog circuits using industry-standard Electronic Design Automation (EDA) tools. Students are expected to develop a comprehensive understanding of schematic capture, layout design, and verification methodologies as per current CMOS technology standards.

List of Experiments:

Students shall design the schematic diagrams using CMOS logic, generate corresponding layout diagrams, and perform simulation and analysis using the latest CMOS process technology with the aid of **professional-grade EDA tools (Cadence/Synopsys/Mentor Graphics/Tanner/Microwind or any Industry Standard EDA Tools)**.

The following experiments shall be carried out:

1. Design and implementation of an inverter.
2. Design and implementation of universal gates.
3. Design and implementation of full adder.
4. Design and implementation of full Subtractor.
5. Design and implementation of RS-latch.
6. Design and implementation of D-latch.
7. Design and implementation asynchronous counter.
8. Design and Implementation of static RAM cell.
9. Design and Implementation of differential amplifier.
10. Design and Implementation of ring oscillator.

Equipment Required:

1. Cadence/Synopsys/Mentor Graphics/Tanner/Microwind or any Industry Standard EDA Tools.
2. Personal computer with necessary peripherals.

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III Year II Semester	MICROPROCESSOR AND MICROCONTROLLERS LAB (BT24EC3205)	L	T	P	C
		0	0	3	1.5

List of Experiments:

PART- A: (Minimum of 5 Experiments has to be performed) 8086 Assembly Language Programming and Interfacing

1. Programs for 16 -bit arithmetic operations (using Various Addressing Modes).
   a. Addition and subtraction of n-BCD numbers.
   b. Multiplication and Division operations.
   c. Addition of an array of numbers with overflow detection.
2. Program for sorting an array.
3. Program for Factorial of given n-numbers.
4. Interfacing ADC to8086
5. Interfacing DAC to8086.
6. Interfacing stepper motor to8086.
7. Interfacing Seven-Segment display to 8086.
8. Keyboard interface with 8086.

PART-B: (Minimum of 5 Experiments has to be performed) 8051 Assembly Language Programming and Interfacing

1. Finding number of 1's and number of 0's in a given 8-bit number
2. Average of n-numbers.
3. Program and verify Timer/ Counter in8051.
4. Interfacing Traffic Light Controller to8051.
5. UART operation in8051
6. Interfacing LCD to8051.
7. Interfacing temperature sensor (LM 35) with 8051.
8. Stepper motor control with 8051.

PART-C (Minimum of 2 Experiments has to be performed) Conduct the following experiments using ARM CORTEX M3 PROCESSOR USING KEIL MDK ARM

1. Write an assembly program to multiply of 2 16-bit binary numbers.
2. Write an assembly program to find the sum of first 10 integers numbers.
3. Write a program to toggle LED every second using timer interrupt.
4. PWM signal generation.
5. Analog signal measurement (ADC).
6. Interfacing with serial communication (UART).

Equipment Required:

1. Regulated Power supplies.
2. Analog/Digital Storage Oscilloscopes.
3. 8086 Microprocessor kits.
4. 8051 microcontroller kits.
5. ADC module, DAC module.
6. Stepper motor module.
7. Key board module.
8. LED, 7-SegemtUnits, LCD display modules.
9. Temperature sensor module.
10. Digital Multimeters.
11. ROM/RAM Interface module.
12. Bread Board etc.
13. ARM CORTEX M3.
14. KEIL MDKARM, Digital Multi-meters.

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III Year II Semester	MACHINE LEARNING LAB (BT24EC3206)	L	T	P	C
		0	1	2	2

Course Objectives:

The main objectives of the course are to

- Make use of Data sets in implementing the machine learning algorithms.
- Implement the machine learning concepts and algorithms in any suitable language of choice.
- Design Python programs for various Learning algorithms.
- Apply supervised learning algorithms including decision trees and k-nearest neighbours (k-NN), SVM and PCA.

List of Experiments:

Requirements: Develop the following program using Anaconda/Jupiter/Spider and evaluate ML models.

Experiment-1:

Implement and demonstrate the FIND-S algorithm for finding the most specific hypothesis based on a given set of training data samples. Read the training data from a .CSV file.

Experiment-2:

For a given set of training data examples stored in a .CSV file, implement and demonstrate the Candidate-Elimination algorithm to output a description of the set of all hypotheses consistent with the training examples.

Experiment-3:

Write a program to demonstrate the working of the decision tree based ID3 algorithm. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample.

Experiment-4:

Exercises to solve the real-world problems using the following machine learning methods:
a) Linear Regression b) Logistic Regression c) Binary Classifier.

Experiment-5: Develop a program for Bias, Variance, Remove duplicates, Cross Validation

Experiment-6: Write a program to implement Categorical Encoding, One-hot Encoding

Experiment-7:

Build an Artificial Neural Network by implementing the Back propagation algorithm and test the same using appropriate data sets.

Experiment-8:

Write a program to implement k-Nearest Neighbor algorithm to classify the iris data set. Print both correct and wrong predictions.

Experiment-9: Implement the non-parametric Locally Weighted Regression algorithm in order to fit data points. Select appropriate data set for your experiment and draw graphs.

Experiment-10:
Assuming a set of documents that need to be classified, use the naïve Bayesian Classifier model to perform this task. Built-in Java classes/API can be used to write the program. Calculate the accuracy, precision, and recall for your data set.

Experiment-11: Apply EM algorithm to cluster a Heart Disease Data Set. Use the same data set for clustering using k-Means algorithm. Compare the results of these two algorithms and comment on the quality of clustering. You can add Java/Python ML library classes/API in the program.

Experiment-12: Exploratory Data Analysis for Classification using Pandas or Matplotlib.

Experiment-13:
Write a Python program to construct a Bayesian network considering medical data. Use this model to demonstrate the diagnosis of heart patients using standard Heart Disease Data Set.

Experiment-14:
Write a program to Implement Support Vector Machines and Principle Component Analysis.

Experiment-15:
Write a program to Implement Principle Component Analysis.

Text Books:

1. "Machine Learning Theory and Practice", M N Murthy, V S Ananthanarayana, Universities Press (India), 2024.

Reference Books:

1. "Machine Learning", Tom M. Mitchell, McGraw-Hill Publication, 2017.
2. "Machine Learning in Action", Peter Harrington, Dream Tech.
3. "Introduction to Data Mining", Pang-Ning Tan, Michel Stenbach, Vipin Kumar, 7th Edition, 2019.

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III Year II Semester	RESEARCH METHODOLOGY AND IPR (BT24HS3101)	L	T	P	C
		2	0	0	0

Course Outcomes:

- Understand research problem formulation.
- Analyze research related information, Follow research ethics.
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand research methodology, ethical practices, and intellectual property rights (IPR) to support innovation and scientific investigation.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

CO-PO/PSO MATRIX: (Level of Mapping- 3: High; 2: Moderate; 1-Low; -: Not mapped)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	3	1	2	-	-	-	-	-	-	-	1	1	-
CO2	-	2	-	3	1	-	-	3	-	2	-	2	1	-
CO3	1	-	-	-	3	2	2	-	-	-	-	3	2	2
CO4	-	-	-	-	-	2	-	2	-	-	2	3	3	2
CO5	2	2	2	3	1	-	-	3	1	2	1	2	2	1
CO6	-	-	-	-	-	2	2	2	-	-	3	2	2	1

Unit 1 :

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem, Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

Unit 2:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

Unit 3:
Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 4:
Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent information and databases, Geographical Indications.

Unit 5:
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc, Traditional knowledge Case Studies, IPR and IITs

TEXT BOOKS
1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineering students'".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS
1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step-by-Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
3. Mayall , "Industrial Design", McGraw Hill,1992

e- Resources: -

- https://www.wipo.int/about-ip/en/
- https://nptel.ac.in/courses/121/101/121101018
- https://ocw.mit.edu/courses/sloan-school-of-management/15-566j-communication-for-engineering-leaders-fall-2005/

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DR24
B.Tech
Honors & Minors

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HONORS:

The following points may be considered to choose appropriate theory and laboratories to obtain B.Tech (Honors).

- The student has to opt for any of the Six subjects / Five Theory and Two laboratories with the approval of the University BoS Chairman.
- Further, if any of these subjects are opted as Open Electives or Program Electives then such Subjects should not be considered to obtain the B.Tech (Honors).
- The student can opt for the NPTEL/SWAYAM online Courses with 12 weeks/16 weeks duration and also with Proctored Examinations.
- Further, the student has to take permission for such NPTEL/SWAYAM Courses from the University BoS Chairman.
- In addition to the program elective given in Regular Courses &Structure, the following subjects are also included, that can be opted for B.Tech (Honors)
- In case of Laboratories, student may opt for virtual Laboratories only with the permission from chairman BoS.
- It is recommended to choose the laboratories along with pre-requisite theory subjects is mandatory

S.No.	Subject	Course Code	L-T-P	Credits
1	Advanced Communications	BT24EC0H01	3-0-0	3
2	EMI/EMC	BT24EC0H02	3-0-0	3
3	VLSI Signal Processing	BT24EC0H03	3-0-0	3
4	CMOS Mixed Signal Design	BT24EC0H04	3-0-0	3
5	Adaptive Signal Processing	BT24EC0H05	3-0-0	3
6	RTOS	BT24EC0H06	3-0-0	3
7	PC based Data Acquisition Systems	BT24EC0H07	3-0-0	3
8	Digital Control Systems	BT24EC0H08	3-0-0	3
9	Microstrip Antennas	BT24EC0H09	3-0-0	3
10	Image & Video Processing	BT24EC0H10	3-0-0	3
11	Swayam 12-week MOOC course-1	BT24EC0H11	3-0-0	3
12	Swayam 12-week MOOC course-2	BT24EC0H12	3-0-0	3
13	Swayam 12-week MOOC course-3	BT24EC0H13	3-0-0	3
14	Advanced Communications Lab	BT24EC0H14	0-0-3	1.5
15	CMOS Mixed Signal Design Lab	BT24EC0H15	0-0-3	1.5
16	RTOS Lab	BT24EC0H16	0-0-3	1.5
17	Digital Control Systems Lab	BT24EC0H17	0-0-3	1.5
18	Antennas and Microwave Lab	BT24EC0H18	0-0-3	1.5
19	Image & Video Processing Lab	BT24EC0H19	0-0-3	1.5
Student shall take up at least TWO NPTEL/SWAYAM of 12-week duration for 3 credits.				

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MINOR:

Student can choose any SIX Theory or any FIVE theory and TWO Laboratories in the list given below which are not chosen as Open electives/in Regular Courses, are to be considered for Minor Degree. Prior Approval BoS Chairman is required

S.No.	Subject	Course Code	L-T-P	Credits
1	Electronics Devices and Basic Circuits	BT24EC0M01	3-0-0	3
2	Digital Electronics	BT24EC0M02	3-0-0	3
3	Principles of Communication	BT24EC0M03	3-0-0	3
4	Signal Analysis	BT24EC0M04	3-0-0	3
5	Microcontrollers and Applications	BT24EC0M05	3-0-0	3
6	Embedded System Design	BT24EC0M06	3-0-0	3
7	Internet of things	BT24EC0M07	3-0-0	3
8	Digital Signal Processing	BT24EC0M08	3-0-0	3
9	Swayam 12-week MOOC course-1	BT24EC0M09	3-0-0	3
10	Swayam 12-week MOOC course-2	BT24EC0M10	3-0-0	3
11	Swayam 12-week MOOC course-3	BT24EC0M11	3-0-0	3
12	Electronics Devices and Basic Circuits LAB	BT24EC0M12	0-0-3	1.5
13	Digital Electronics LAB	BT24EC0M13	0-0-3	1.5
14	Internet of things LAB	BT24EC0M14	0-0-3	1.5
15	Digital Signal Processing LAB	BT24EC0M15	0-0-3	1.5
Student shall take up at least ONE NPTEL/SWAYAM of 12-week duration for 3 credits.				

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Honor Course	ADVANCED COMMUNICATIONS (BT24EC0H01)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:
- Learn 5G Technology advances and their benefits
- Learn the key MIMO, SDR changes required to support 5G
- Learn Device to device communication with Wireless Networks
- Implementation options for 5G

UNIT I:
SPREAD SPECTRUM AND MULTIPLE ACCESS TECHNIQUES: Introduction, Pseudo noise sequence, DS spread spectrum with coherent binary PSK, processing gain, FH spread spectrum, multiple access techniques wireless communication, TDMA and CDMA in wireless communication systems, source coding of speech for wireless communications.

UNIT II:
Wireless channel modeling (microwave, mmWave, and teraHertz): Propagation mechanism, reflection, refraction, diffraction and scattering. Fading channels- Multipath and small-scale fading Doppler shift, statistical multipath channel models, narrowband and wideband fading models, coherence bandwidth, and coherence time.

UNIT III:
Multiple-Input, Multiple-Output (MIMO) wireless communication: Basic MIMO model, MIMO capacity in fading channels, Diversity multiplexing trade off, Space-time code for MIMO wireless communication.
Software Define Radio (SDR): Characteristics and benefits of a software radio, design principles of software radio, enhanced flexibility with software radios, receiver design challenges.

UNIT IV:
Wireless Networks Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11, IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL

UNIT V:
5G Communication: 5G spectrum landscape and requirements, Spectrum access modes and sharing scenarios, 5G spectrum technologies. 5G CHANNEL MODEL: The 5G wireless Propagation Channels: Channel modeling requirements, propagation scenarios and challenges in the 5G modeling. 5G USE CASES AND SYSTEM CONCEPT: Use cases and requirements, 5G system concept.5G waveforms, OFDM, OTFS, OFDMA, carrier aggregation, dual connectivity. Beyond 5G key enablers: Intelligent reflecting surfaces (IRS), wireless energy harvesting, SWIPT, integrated sensing and communication

Text Books:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. S. Haykin and M. Moher, Modern Wireless Communication, Pearson Education, 2005.
3. Jeffrey H. Reed, Software Radio: A Modern Approach to Radio Engineering, Prentice Hall, May 2002

References Books:

1. C. Oestges and B. Clerckx, MMIO Wireless Communications, 1st Ed, 2007.
2. Paul Burns, Software Defined Radio for 3G, Artech House Inc., 2003.
3. Afif Osseiran, Jose F Monserrat, Patrick Marsch, "5G Mobile and Wireless Communications Technology", Cambridge University Press, 2016
4. Wireless Sensor Networks: An Information Processing Approach, 1st edition, Feng Zhao, Leonidas Guibas, Elsevier Science imprint, Morgan Kauffman Publishers, 2005, rp2009

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Honor Course	EMI/EMC (BT24EC0H02)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Discuss effects of EMI and counter measures by EMC-techniques.
- Apply the knowledge gained in selecting proper gadget/device/appliance/system, as per EMC- norms specified by regulating authorities.
- Students shall choose career in the fields of EMI/EMC as an Engineer /Researcher /Entrepreneur in India/abroad.
- Understand the various aspects of shielding & PCB Tracing, termination& Implementation
- Identifying of EMI Hotspot and various techniques like grounding filtering soldering etc

UNIT – I:

Natural and Nuclear sources of EMI / EMC: Introduction, Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations. An overview of EMI/ EMC, Natural and Nuclear sources of EMI

UNIT – II:

EMI from apparatus, circuits and open area test sites: Electromagnetic emissions, noise from relays and switches, non-linearity in circuits, passive inter-modulation, cross talk in transmission lines, transients in power supply lines, electromagnetic interference (EMI). Open area test sites and measurements.

UNIT – III:

Radiated and conducted interference measurements: Anechoic chamber, TEM cell, GH TEM Cell, characterization of conduction currents / voltages, conducted EM noise on power lines, conducted EMI from equipment, Immunity to conducted EMI detectors and measurements.

UNIT – IV:

ESD, Grounding, shielding, bonding and EMI filters: Principles and types of grounding, shielding and bonding, characterization of filters, power lines filter design. ESD, Electrical fast transients / bursts, electrical surges.

UNIT – V:

Cables, connectors, components: Introduction, EMI suppression cables, EMC connectors, EMC gaskets, Isolation transformers, optoisolators, Transient and Surge Suppression Devices.

EMC standards- National / International: Introduction, Standards for EMI and EMC, MIL-Standards, IEEE/ANSI standards, CISPR/IEC standards, FCC regulations, EMI/EMC standards in JAPAN, Conclusions.

Text Books:

1. Engineering Electromagnetic Compatibility by Dr. V.P. Kodali, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.

References Books:

1. Introduction to Electromagnetic Compatibility, NY, John Wiley, 1992, by C.R. Pal.
2. Electromagnetic Interference and Compatibility IMPACT series, IIT – Delhi.

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Honor Course	VLSI SIGNAL PROCESSING (BT24EC0H03)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Understand Pipelining, and parallel processing.
- Use VLSI design for digital filters
- Optimize VLSI architectures for basic DSP algorithms
- Analyze various parallel processing algorithms
- Be familiar with VLSI algorithms and architectures for DSP.
- Be able to implement basic architectures for DSP using CAD tools

UNIT-I:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms. **Pipelining and Parallel Processing:** Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power. **Retiming:** Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II:

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III:

Systolic Architecture Design

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV:

Fast Convolution

Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V:

Low Power Design

Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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Honor Course	CMOS MIXED SIGNAL DESIGN (BT24EC0H04)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Appreciate the fundamentals of data converters and also optimized their performances.
- Understand the design methodology for mixed signal IC design
- Analyze the design of PLL and operational amplifiers
- Design the CMOS digital circuits and implement its layout.
- Design the Switched Capacitor Circuits for different applications.

UNIT-I: Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II: Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III: Data Converter Fundamentals

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV: Nyquist Rate A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V: Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2016
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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Honor Course	ADAPTIVE SIGNAL PROCESSING (BT24EC0H05)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Review the Adaptive Systems and Understand the various measures to be opted for developing adaptive systems
- Understand different algorithms to develop the adaptive filtering
- Apply adaptive filter theory for different problems
- Perform RLS & Kalman Filtering

Unit -I

Introduction to Adaptive Systems: Adaptive Systems: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner - Description, Weight Vectors, Desired Response, Performance function - Gradient & Mean Square Error.

Unit-II

Development of Adaptive Filter Theory & Searching the Performance surface: Introduction to Filtering - Smoothing and Prediction – Linear Optimum Filtering, Problem statement, Principle of Orthogonality - Minimum Mean Square Error, Wiener- Hopf equations, Error Performance surface Searching the performance surface – Methods & Ideas of Gradient Search methods, Gradient Searching Algorithm & its Solution, Stability& Rate of convergence, Learning Curve.

Unit-III

Steepest Descent Algorithms: Gradient Search by Newton's Method, Method of Steepest Descent, Comparison of Learning Curves.

Unit-IV

LMS Algorithm & Applications: Overview - LMS Adaptation algorithms, Stability &Performance analysis of LMS Algorithms - LMS Gradient & Stochastic algorithms -Convergence of LMS algorithm. Applications: Noise cancellation – Cancellation of Echoes inlong distance telephone circuits, Adaptive Beam forming.

Unit-V

RLS &Kalman Filtering: Introduction to RLS Algorithm, Statement of Kalman filtering problem, The Innovation Process, Estimation of State using the Innovation Process- Expression of Kalman Gain, Filtering Examples using Kalman filtering.

Text Books

1. Adaptive Signal Processing - Bernard Widrow, Samuel D. Streams, 2005, PE.
2. Adaptive Filter Theory - Simon Haykin-, 4th Ed., 2002, PE Asia.

Reference Books

1. Optimum signal processing: An introduction – Sophocles. J. Orfamadis, 2nd Ed., 1988, McGraw-Hill, New York
2. Adaptive signal processing-Theory and Applications - S. Thomas Alexander, 1986, Springer – Verlag.
3. Signal analysis – Candy, McGraw Hill Int. Student Edition
4. James V. Candy - Signal Processing: A Modern Approach, McGraw-Hill, International Edition, 1988

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Honor Course	RTOS (BT24EC0H06)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- List the mathematical model of the system and to develop real time algorithm for task scheduling.
- Categorize capabilities Handling Resource Sharing and dependencies among Real-time Tasks generate a high-level analysis for Scheduling Real-time tasks in multiprocessor and distributed systems
- Analyze the working of real time operating systems and real time database.
- Apply the fault tolerance techniques, evaluation of reliability.

UNIT-I: Introduction

OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-II: RTOS Programming

Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-III: Program Modeling – Case Studies

case study of digital camera hardware and software architecture, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-IV: Target Image Creation & Programming in Linux

Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming

UNIT-V: Programming in RT Linux

Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System

TEXT BOOKS:

1. Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008.
2. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, 2005 Edition, Black pad book.

REFERENCES:

1. Labrosse, "Embedding system building blocks ", CMP publishers.
2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

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Honor Course	PC BASED DATA ACQUISITION SYSTEMS (BT24EC0H07)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Be able to identify a data acquisition system, objectives and different configurations
- Be familiar with different methods of linear/Nonlinear Analog-to-Digital conversion and their role in real time applications
- Be familiar with different methods of linear/Nonlinear Digital to Analog Conversion. and their role in real time applications
- Be able to identify the type of interface used to get a digital signal/Analog signal into a microprocessor and familiar with Monolithic Converters.
- Be familiar with different noise reduction techniques in DAS and case studies of Data Converter

UNIT-I

INTRODUCTION: Objective of a DAS, single channel DAS, Multi-channel DAS, Components used in DAS– Converter Characteristics-Resolution-Non-linearity, settling time, Monotonicity.

UNIT-II

ANALOG TO DIGITAL CONVERTERS (ADCS): Classification of A/D converters. Parallel feedback – Successive approximation – Ramp comparison – Dual slope integration – Voltage to frequency – Voltage to Time – Logarithmic types of ADCS.

NON-LINEAR DATA CONVERTERS (NDC): Basic NDC configurations – Some Common NDACS and NADCS – Programmable non-linear ADCS – NADC using optimal sized ROM –High speed hybrid NADC – PLS based NADC – Switched capacitor NDCS.

ADC APPLICATIONS: Data Acquisition systems – Digital signal processing systems –PCM voice communication systems – Test and measurement instruments – Electronic Weighing machines.

UNIT-III

DIGITAL TO ANALOG CONVERTERS (DACS): Principles and design of – Parallel R–2R, Weighted resistor, inverted ladder, D/A decoding – Codes other than ordinary binary.

DATA CONVERTER APPLICATIONS: DAC applications – Digitally programmable V/I sources – Arbitrary waveform generators – Digitally programmable gain amplifiers – Analog multipliers/ dividers – Analog delay lines.

UNIT-IV

Monolithic data converters: typical study of monolithic DACS and ADCS. Interfacing of DACS and ADCS to a μP.

UNIT-V

Error budget of DACS and ADCS: Error sources, error reduction and noise Reduction techniques in DAS. Error budget analysis of DAS, case study of a DAC and an ADC.

TEXT BOOKS:

1. Electronic data converters fundamentals and applications – Dinesh K. Anvekar, B.S. Sonde –Tata McGraw Hill.

REFERENCES:

1. Electronic Analog/ Digital conversions – Hermann Schmid – Tata McGraw Hill.
2. E.R. Hanateck, User's Handbook of D/A and A/D converters - Wiley
3. Electronic instrumentation by HS Kalsi- TMH 2 ndEdition, 2004.
4. Data converters by G.B. Clayton

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Honor Course	DIGITAL CONTROL SYSTEMS (BT24EC0H08)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Have the awareness of Discrete Time Control Systems
- Calculate the Z-transforms and use its concepts of Discrete control systems
- Get familiarize with design of Discrete control systems using various Approaches
- Understand the State Space approach to analyze the discrete system
- Have the concepts of Controllability and Observability of discrete control system

UNIT –I: Introduction to Discrete Time Control Systems:
Introduction, Digital Control Systems, Quantizing and Quantization Error, Data Acquisition, Conversion, and Distribution Systems

UNIT-II:
The Z – Transforms:
Introduction, The Z Transform, Z-Transform of elementary functions, properties and theorems of Z-Transform, Inverse Z-Transform, Z-Transform method for solving difference equations
Z-Plane Analysis of Discrete-Time Control System:
Introduction, Impulse Sampling and Data Hold, Obtaining the Z-Transform by the convolutional integral method, Reconstruction of original signals from sampled signals, Pulse transfer function, Realization of digital controllers and digital filters

UNIT –III: Design of Discrete Time Control Systems by Conventional Methods:
Introduction, Mapping between the s plane and the z plane, stability analysis of closed loop systems in the z plane, transient and steady response analysis, design based on the Root-Locus method, design based on the frequency response method, Analytical design method.

UNIT-IV: State Space Analysis:
Introduction, State Space Representation of discrete time systems, solving discrete time state space equations, Pulse Transfer function matrix, Discretization of continuous time state – space equations, Liapunov stability analysis

UNIT –V: Controllability and Observability:
Introduction, Controllability, Observability, Useful Transformations in State Space Analysis and Desig.

TEXT BOOKS:

1. K. Ogata - "Discrete-Time Control systems" - Pearson Education/PHI, 2nd Edition.

REFERENCE BOOKS:

1. Kuo - "Digital Control Systems"- Oxford University Press, 2nd Edition, 2003.
2. M. Gopal - "Digital Control and State Variable Methods"- TMH

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Honor Course	MICROSTRIP ANTENNAS (BT24EC0H09)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Remember the antenna basics and planar antennas.
- Describe and discuss characteristics and principles of microstrip antennas.
- Demonstrate and implement the CP patch antennas and micro strip antenna arrays.
- Analyze planar slot antennas and planar monopole antennas.
- Evaluate characteristics and design aspects of electrically small antennas.
- Investigate planar antennas for special applications for wireless access.

UNIT –I:

Planar Radiators: Introduction to antennas (radiation pattern, directivity, efficiency, gain, impedance, axial ratio etc.), different types of planar antennas, applications of planar antennas, Brief description of fabrication process of planar antennas.

UNIT –II:

Microstrip Patch Antennas-I: Characteristics of microstrip patch antennas, radiation from microstrip antenna, field configurations, different types of feeding techniques. Design equations for rectangular and circular microstrip patches, analysis of microstrip antennas using transmission line model and cavity method. Broadband techniques using stacked patch antennas, proximity- coupled and aperture-coupled microstrip antennas, slot-loaded and slit-loaded microstrip antennas, microstrip antennas with shorted pin, effect of finite ground plane on the performance of microstrip antennas, principle of planar fractal antennas.

UNIT –III:

Microstrip Patch Antennas-II: Methods of generating circular polarization in microstrip antennas using single feed and double feed, methods of generating multiple frequencies using microstrip antennas, miniaturization techniques for mcirostrip antennas. Design techniques of microstrip antenna arrays with feed network, effect of mutual coupling, microstrip phased array antenna design.

UNIT –IV:

Planar Slot Antennas: Geometry and design of microstrip slot antenna, radiation pattern, CPW-fed slot antennas, design of folded slot antenna, annular slot antenna.

Planar Monopole Antennas: Feeding methods and characteristics of planar triangle monopole, Sierpinski monopole, planar bi-conical monopole antenna and roll monopole antenna.

UNIT –V:

Planar Antennas for Special Applications: Planar mobile handset antennas, planar laptop computer antennas, planar antennas for USB modem, planar antennas for WLAN and UWB communication.

TEXT BOOKS:

1. Ramesh Garg, Prakash Bhartia, Inder Bahl, Apisak Ittipiboon 'Microstrip Antenna Design Handbook, Artech House, 2001.
2. K. F. Lee and W. Chen 'Advances in Microstrip and Printed Antennas, John Wiley & Sons, 1997.
3. R. Bancroft 'Microstrip and Printed Antenna Design, SciTech Publishing, 2nd Edition, 2009.

REFERENCES:

1. S. Maci and G. Biffi Gentili Printed Antennas for Wireless Communications, IEEE Press, 1997.
2. Ahmed A. Kishk, Kai-Fong Lee, Samir A. Makarov 'Antenna Fundamentals for Legacy Mobile Applications and Beyond, Springer, 2016.
3. Antennas – John D. Kraus, McGraw-Hill, 2nd Edition, 1988.

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Honor Course	IMAGE & VIDEO PROCESSING (BT24EC0H10)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Describe the Image Processing system, scope of digital image processing and compare various image transforms.
- Apply filtering operations on images both in spatial and frequency domain; describe image restoration in presence of noise and degradation.
- Analyze various segmentation techniques and compression methods on digital images.
- Describe the fundamental of digital video, sampling and filtering of video signals.
- Explain various methods for two-dimensional motion estimation and their applications in video processing

Unit – I

Introduction: Introduction to Image Processing, Examples of fields that use Digital Image Processing, Fundamental steps in digital image processing, components of an image processing system, Examples of the fields that use Digital Image Processing. Image sensing and acquisition, image sampling and quantization, Some basic relationships between pixels.

Image Transforms: Need for image transforms, Image transforms, Fourier Transform, 2D Discrete Fourier Transform and its properties, Walsh Transform, Hadamard transform, Haar Transform, Slant transform, Discrete Cosine transform, KL Transform, Singular Value Decomposition.

Unit – II

Image Enhancement:

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, smoothing spatial filters, Sharpening spatial filters.

Filtering in frequency domain: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Restoration:

A model of the image degradation / Restoration process, Noise models, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.

Unit – III

Image segmentation: Fundamentals, point, line, edge detection, thresholding, and Region –based segmentation. Image compression: Fundamentals, Basic compression methods: Huffman coding, Golom bcoding, Arithmetic coding, LZW coding, Run-Length coding, Block Transform coding, Predictive coding.

Unit – IV

Basic Steps of Video Processing:

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

Unit – V

2-D Motion Estimation:

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Digital Video Processing – M. Tekalp, Prentice Hall International.
3. Video Processing and Communication – Yao Wang, JoemOstermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:

1. Fundamentals of Digital Image Processing – Anil K. Jain, Prentice Hall of India, 9th Edition, Indian Reprint, 2002.
2. Digital Image Processing –S. Jayaraman, S. Esakkirajan, and T. Veerakumar, McGraw-Hill Education, 2018.

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Honor Course	ADVANCED COMMUNICATIONS LAB (BT24EC0H14)	L	T	P	C
		0	0	3	1.5

List of Experiments :(Minimum of Twelve Experiments has to be performed)

1. Implementation of Linear Block Code Encoder and Decoder
2. Implementation of Binary Cyclic Codes Encoder and Decoder
3. Implementation of Convolution Encoder- Decoder
4. Determination of Losses in Optical Fiber
5. Characteristics of LASER Diode.
6. Study of Satellite Communication System, uplink transmitter, down link receiver and transponder
7. Signal to noise ratio and Link Failure operations in satellite communication
8. Carrier to Noise Ratio in Satellite Communication
9. Study of Direct Sequence Spread Spectrum Modulation & Demodulation using CDMA-DSS BER Trainer
10. Efficiency of DS Spread- Spectrum Technique
11. Simulation of Frequency Hopping (FH) system
12. Generation of PN sequence and Gold Sequence
13. Outdoor propagation model - Okumura model and Hata model
14. Free space propagation – path loss model
15. Study of WLAN / network topologies

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Honor Course	CMOS MIXED SIGNAL DESIGN LAB (BT24EC0H15)	L	T	P	C
		0	0	3	1.5

List of Experiments:

Cycle 1:
1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   i. Two stage cross coupled clamped comparator ii. Strobed Flip-flop
3) Data converter

Cycle 2:
1) Switched capacitor circuits i. Parasitic sensitive integrator ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

Lab Requirements:

Software: Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools
Hardware: Personal Computer with necessary peripherals, configuration and operating System.

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Honor Course	RTOS Lab (BT24EC0H16)	L	T	P	C
		0	0	3	1.5

- The students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.
- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments:

Part-I: Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II: Experiments on ARM-CORTEX processor using any open source RTOS.
(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
- LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

- The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
- Serial Cables, Network Cables and recommended power supply for the board.

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Honor Course	DIGITAL CONTROL SYSTEMS LAB (BT24EC0H17)	L	T	P	C
		0	0	3	1.5

1. To study

   a. Conversion of a transfer function from continuous domain to discrete domain.
   b. Conversion of a transfer function from the continuous domain to the digital domain.
   c. Pole Zero Map of a discrete transfer function

2. To determine

   a. Z transform of a discrete-time signal
   b. Inverse Z transform of a discrete-time signal
   c. Factored form and partial fraction form of a rational z function d. Pole zero map of a digital system

3. To study

   a. Closed loop response of a discrete-time system
   b. Comparison of time responses of continuous time and discrete time systems
   c. Effect of sampling time on system response and system parameters

4. To design a lead compensator to obtain system response with the desired accuracy, and less overshoot.

5. To design a lag compensator to meet performance specification parameters

6. To study a. The effect of variation in controller parameters on system response

7. To obtain

   a. Transfer function model from a state model
   b. State model from transfer function model
   c. Step response of a system represented by its state model

8. To determine

   a. Eigenvalues from state model
   b. Eigenvalues from transfer function model
   c. Stability of a system

9. To study the effect of common nonlinearities such as relay, dead zone, and saturation on the response of a 2nd order control system

Softwares Required

1. Matlab Software
2. Simulink Tool

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Honor Course	ANTENNAS and MICROWAVE LAB (BT24EC0H18)	L	T	P	C
		0	0	3	1.5

LIST OF EXPERIMENTS: (Minimum of Ten Experiments has to be performed)

1. Calculation of transmission line parameters (R, L, G and C) for two wire line, coaxial line and Strip line.
2. Study on the standing wave pattern along a transmission line when the line is open-circuited, Short circuited and terminated by a resistive load at the load end.
3. Investigate the effect of length of transmission line on the input impedance at the sending end.
4. Familiarization of Smith chart on MATLAB platform.
5. Radiation resistance of electric and magnetic dipoles as a function of electrical size.
6. Feed (input terminal) impedance of an electric dipole as a function of antenna length.
7. 3D radiation pattern of a half-wavelength dipole antenna in both horizontal and vertical Orientations
8. Radiation patterns for electric dipoles of various electrical lengths.
9. Characteristics and radiation patterns of Linear array, Planar and Circular arrays.
10. Variation of normalized input impedance with Feeding position in Inset-Fed Microstrip patch Antenna
11. Design of Rectangular Microstrip Patch antenna.

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Honor Course	IMAGE & VIDEO PROCESSING LAB (BT24EC0H19)	L	T	P	C
		0	0	3	1.5

List of Experiments:

Note: In the first 10 experiments, atleast 8 experiments; In the last three experiments, atleast 2 experiments must be executed.

1. Perform basic operations on images like addition, subtraction etc.
2. Perform Pixel based operations (Point based operations) for Image enhancement
3. Plot the histogram of an image and perform histogram equalization
4. Filtering in Spatial Domain
5. Computation of 2D-DFT and Perform filtering in Frequency domain
6. Implementation of Image Restoration methods
7. Implementation of JPEG compression Algorithm (Without using Library function)
8. Comparison of coding Techniques for image compression (Bit plane, Predictive, Arithmetic, Huffman coding).
9. Detections of edges in an image (Prewitt, Sobel, Krisch and Laplacian of Gaussian Operators, Canny operators) and compare
10. Image Segmentation based on thresholding.
11. Basic operations on Video, and identification of key frame
12. Computation of optical flow velocities for a moving object in a Video
13. Implementation of two-dimensional motion estimation

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		L	T	P	C
Minor Course	**ELECTRONICS DEVICES AND BASIC CIRCUITS (BT24EC0M01)**	**3**	**0**	**0**	**3**

COURSE OUTCOMES:

- Understand the semiconductor physics, their concepts and characteristics of p-n junction diode.
- Understand V-I characteristics of various semiconductor devices.
- Learn the operation of transistor and its characteristics in various configurations, Biasing of transistor
- Analyze the transistor using h-parameters and its equivalent model.
- Describe the operation of FET and MOSFET, their application as an amplifier.

UNIT I:

Review of Semiconductor Physics: Mobility and Conductivity, Intrinsic and extrinsic semiconductors, Hall effect

Junction Diode Characteristics: Energy band diagram of PN junction Diode, Open circuited p-n junction, Biased p-n junction, p-n junction diode, current components in p-n junction Diode, Qualitative explanation of Diode equation (Derivation not required) , V-I Characteristics, temperature dependence on V-I characteristics, Diode resistance, Diode capacitance

UNIT II:

Special Semiconductor Devices: Zener Diode, Breakdown mechanisms, Zener diode applications, Varactor Diode, LED, Photodiode, Tunnel Diode and its characteristics with the help of energy band diagram, UJT and its application, PNPN Diode, SCR, Construction, operation and V-I characteristics.

Diode Circuits: Clipping (limiting) circuits, Peak Detector, Clamping circuits, Comparators, Basic Rectifier setup, half wave rectifier, full wave rectifier, bridge rectifier, Inductor filter, Capacitor filter

UNIT III:

Transistor Characteristics: Junction transistor, transistor current components, transistor equation in CB configuration, transistor as an amplifier, characteristics of transistor in Common Base and Common Emitter configurations, punch through/ reach through, typical transistor junction voltage values.

Transistor Biasing and Thermal Stabilization : Need for biasing, operating point, load line analysis, BJT biasing- methods, basic stability, fixed bias, collector to base bias, self bias, Stabilization against variations in V_{BE}, Ic, and β, Stability factors, (S,S',S''), Bias compensation, Thermal runaway, Thermal stability.

UNIT IV:

Small Signal Low Frequency Transistor Amplifier Models

BJT: Two port network, Transistor hybrid model, determination of h-parameters, Millers theorem and Dual of Millers theorem, Analysis of CB, CE and CC amplifiers using exact analysis, Comparison of transistor amplifiers.

UNIT V:

FET: FET types, JFET operation and characteristics (qualitative explanation only), small signal model of JFET.

MOSFET: MOSFET Structure, Operation of MOSFET, MOSFET as a variable resistor, derivation of V-I characteristics of MOSFET, Comparison of Bipolar and MOS devices.

CMOS amplifiers: General Considerations, Common Source Stage, Common Gate Stage, Source Follower, comparison of FET amplifiers.

Text Books:

1. Electronic Devices and Circuits- J. Millman, C. C. Halkias, Mc-Graw Hill Education.
2. Integrated Electronics-J. Millman, C. Halkias, Mc-Graw Hill Education.
3. Fundamentals of Microelectronics-Behzad Razavi, Wiley, 3rd edition, 2021.

References:

1. Electronics devices & circuit theory- Robert L.Boylestad and LouiNashelsky, Pearson, 11th edition, 2015.
2. Electronic Devices and Circuits - David A. Bell, Oxford University Press, 5th edition, 2008.
3. Electronic Devices and Circuits- S. Salivahanan, N. Suresh Kumar, Mc-Graw Hill, 5th edition, 2022.

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Minor Course	DIGITAL ELECTRONICS (BT24EC0M02)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

a. Classify different number systems and apply to generate various codes.
b. Use the concept of Boolean algebra in minimization of switching functions
c. Design different types of combinational logic circuits.
d. Apply knowledge of flip-flops in designing of Registers and counters
e. The operation and design methodology for synchronous sequential circuits and algorithmic state machines.
f. Produce innovative designs by modifying the traditional design techniques.

UNIT – I
REVIEW OF NUMBER SYSTEMS & CODES:

Representation of numbers of different radix, conversation from one radix to another radix, r 1's compliments and r's compliments of signed members. Gray code , 4 bit codes; BCD, Excess-3, 2421, 84-2-1 code etc. Error detection & correction codes: parity checking, even parity, odd parity, Hamming code.

UNIT – II
BOOLEAN THEOREMS AND LOGIC OPERATIONS:

Boolean theorems, principle of complementation & duality, De-Morgan theorems. Logic operations ; Basic logic operations -NOT, OR, AND, Universal Logic operations, EX-OR, EX- NOR operations. Standard SOP and POS Forms, NAND-NAND and NOR-NOR realizations, Realization of three level logic circuits. Study the pin diagram and obtain truth table for the following relevant ICs 7400,7402,7404,7408,7432,7486.

MINIMIZATION TECHNIQUES: Minimization and realization of switching functions using Boolean theorems, K-Map (up to 6 variables)and tabular method(Quine-mcCluskey method) with only four variables and single function.

UNIT – III

COMBINATIONAL LOGIC CIRCUITS DESIGN: Design of Half adder, full adder, half subtractor, full subtractor, applications of full adders; 4 bit adder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit and carry look-a-head adder circuit, Design code converts using Karnaugh method and draw the complete circuit diagrams.

COMBINATIONAL LOGIC CIRCUITS DESIGN USING MSI &LSI :

Design of encoder, decoder, multiplexer and de-multiplexers, Implementation of higher order circuits using lower order circuits. Realization of Boolean functions using decoders and multiplexers. Design of Priority encoder, 4-bit digital comparator and seven segment decoder. . Study the relevant ICs pin diagrams and their functions 7442,7447,7485,74154.

UNIT – IV SEQUENTIAL CIRCUITS: Classification of sequential circuits (synchronous and asynchronous), operation of NAND & NOR Latches and flip-flops; truth tables and excitation tables of RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals. Conversion from one flip-flop to another flip-flop. Design of 5ripple counters, design of synchronous counters, Johnson counter, ring counter. Design of registers - Buffer register, control buffer register, shift register, bi directional shift register, universal shift, register.

UNIT-V INTRODUCTION OF PLD's: PLDs: PROM, PAL, PLA -Basics structures, realization of Boolean functions, Programming table. ROM: Internal structure, Static RAM: Internal structure, Dynamic RAM: Internal structure.

TEXT BOOKS:

1. Switching and finite automata theory Zvi.KOHAVI, Niraj.K.Jha 3rd Edition, Cambridge University Press,2009
2. Digital Design by M.Morris Mano, Michael D Ciletti,4th edition publication,2008 PHI
3. Switching theory and logic design by Hill and Peterson, Mc-Graw Hill TMH edition, 2012.

REFERENCES:

1. Fundamentals of Logic Design by Charles H. Roth Jr, Jaico Publishers,2006
2. Digital electronics by R S Sedha.S.Chand& company limited,2010
3. Switching Theory and Logic Design by A. Anand Kumar, PHI Learning pvt ltd,2016.
4. Digital logic applications and design by John M Yarbough, Cengage learning, 2006.

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Minor Course	PRINCIPLES OF COMMUNICATION (BT24EC0M03)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Analyze the performance of analog modulation schemes in time and frequency domains.
- Analyze the performance of angle modulated signals.
- Characterize analog signals in time domain as random processes and noise
- Characterize the influence of channel on analog modulated signals
- Determine the performance of analog communication systems in terms of SNR

UNIT I : Basic tools for communication, Fourier Series/Transform, Properties, Autocorrelation, Energy Spectral Density, Parsevals Relation, Amplitude Modulation (AM), Spectrum of AM, Envelope Detection, Power Efficiency, Modulation Index

UNIT II : Double Sideband Suppressed Carrier (DSB-SC) Modulation, Demodulation, Costas Receiver, Single Sideband Modulation (SSB), Hilbert Transform, Complex Pre-envelope/ Envelope, Demodulation of SSB, Vestigial Sideband Modulation (VSB)

UNIT III : Angle Modulation, Frequency Modulation (FM), Phase Modulation (PM), Modulation Index, Instantaneous Frequency, Spectrum of FM Signals, Carsons Rule for FM Bandwidth, Narrowband FM Generation, Wideband FM Generation via Indirect Method, FM Demodulation

UNIT IV : Introduction to Sampling, Spectrum of Sampled Signal, Aliasing, Nyquist Criterion, Signal Reconstruction from Sampled Signal, Pulse Amplitude Modulation, Quantization, Uniform Quantizers – Midrise and Midtread, Quantization noise, , Non uniform Quantizers, Delta Modulation, Differential Pulse Code Modulation (DPCM)

UNIT V: : Basics of Probability, Conditional Probability, MAP Principle, Random Variables, Probability Density Functions, Applications in Wireless Channels, Basics of Random Processes ,Gaussian Random Process, Noise.

TEXT BOOKS:

1. Simon Haykin, Communications Systems, 4th Edition. John Wiley and Sons, Inc
2. Fundamentals of Wireless Communication by David Tse

References:

1. Principles of Communication Systems – Simon Haykin, John Wiley, 2nd Edition.
2. Electronics & Communication System – George Kennedy and Bernard Davis, TMH 2004.

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Minor Course	SIGNAL ANALYSYS (BT24EC0M04)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- To be able to determine if a given system is linear/causal/stable
- Capable of determining the frequency components present in a deterministic signal
- Capable of characterizing LTI systems in the time domain and frequency domain
- To be able to compute the output of an LTI system in the time and frequency domains

UNIT I: CLASSIFICATION OF SIGNALS AND SYSTEMS

Standard signals- Step, Ramp, Pulse, Impulse, Real and complex exponentials and Sinusoids_ Classification of signals – Continuous time (CT) and Discrete Time (DT) signals, Periodic & Aperiodic signals, Deterministic & Random signals, Energy & Power signals - Classification of systems- CT systems and DT systems- – Linear & Nonlinear, Time-variant & Time-invariant, Causal & Non-causal, Stable & Unstable.

UNIT II: ANALYSIS OF CONTINUOUS TIME SIGNALS Fourier series for periodic signals - Fourier Transform – properties- Laplace Transforms and properties

UNIT III: LINEAR TIME INVARIANT CONTINUOUS TIME SYSTEMS

Impulse response - convolution integrals- Differential Equation- Fourier and Laplace transforms in Analysis of CT systems - Systems connected in series / parallel.

UNIT IV: ANALYSIS OF DISCRETE TIME SIGNALS

Baseband signal Sampling – Fourier Transform of discrete time signals (DTFT) – Properties of DTFT - Z Transform & Properties

UNIT V: LINEAR TIME INVARIANT-DISCRETE TIME SYSTEMS

Impulse response – Difference equations-Convolution sum- Discrete Fourier Transform and Z Transform Analysis of Recursive & Non-Recursive systems-DT systems connected in series and parallel.

TEXT BOOKS:

1. Allan V.Oppenheim, S.Wilsky and S.H.Nawab, —Signals and Systems‖, Pearson, 2015

REFERENCES BOOKS

1. B. P. Lathi, —Principles of Linear Systems and Signals‖, Second Edition, Oxford, 2009.

2. R.E.Zeimer, W.H.Tranter and R.D.Fannin, —Signals & Systems - Continuous and Discrete‖, Pearson,

3. John Alan Stuller, —An Introduction to Signals and Systems‖, Thomson, 2007.

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		L	T	P	C
Minor Course	**MICROCONTROLLERS AND APPLICATIONS (BT24EC0M05)**	**3**	**0**	**0**	**3**

Course Outcomes:

- Understand the architecture and operation of common microcontrollers.
- Write and debug assembly/C programs for microcontrollers.
- Interface microcontrollers with input/output devices.
- Interface microcontrollers with various advanced peripherals.
- Design and implement microcontroller-based applications.

Unit 1: Introduction to Microcontrollers

Evolution of microcontrollers and comparison with microprocessors, Microcontroller families (8051, PIC, AVR, ARM), Architecture of 8051 microcontroller, Memory organization, registers, and flags, Overview of development tools (IDE, simulators, programmers)

Unit 2: Programming of Microcontrollers

Instruction set of 8051, Assembly language programming, Introduction to Embedded C programming, Debugging and simulation tools

Unit 3: Interfacing with Input/Output Devices

Basics of interfacing and role of GPIO, Interfacing LEDs, switches, and push buttons, Interfacing 7-segment displays and buzzers, Interfacing LCDs (16x2 and 20x4, Keypad interfacing for user inputs

Unit 4: Interfacing with Advanced Peripherals and Communication Devices

Interfacing sensors (temperature, light, and proximity sensors), Interfacing actuators (motors: DC, stepper, and servo). Communication interfaces: UART (serial communication with PC), SPI and I2C (interfacing EEPROM and sensors), ADC/DAC interfacing (e.g., analog sensors and audio signals). Interfacing wireless modules (Bluetooth, ZigBee, ESP8266/ESP32 for IoT applications)

Unit 5: Advanced Microcontrollers
Introduction to ARM Cortex-M series, Comparison of ARM with 8051 and PIC, Overview of Arduino and Raspberry Pi platforms, Embedded IoT basics
Real-Time Applications and Case Studies: Microcontroller applications in robotics, automation, and consumer electronics, Designing energy-efficient systems with microcontrollers;
Case studies: Home automation, Smart agriculture systems, Healthcare monitoring.

Textbook:

1. Mazidi and Mazidi, The 8051 Microcontroller and Embedded Systems, 4th Impression, PHI, 2000.
2. Raj Kamal, Microcontrollers Architecture, Programming, Interfacing and System Design, 2nd Edition, Pearson Education, 2005.

Reference Books:

1. Kenneth J. Ayala, *The 8051 Microcontroller: Architecture, Programming, and Applications*, Cengage Learning.
2. John Boxall, *Arduino Workshop: A Hands-On Introduction with 65 Projects*, No Starch Press.

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Minor Course	EMBEDDED SYSTEM DESIGN (BT24EC0M06)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Understand the basic concepts of an embedded system and able to know an embedded system design approach to perform a specific function.
- The hardware components required for an embedded system and the design approach of an embedded hardware.
- The various embedded firmware design approaches on embedded environment.
- Understand how to integrate hardware and firmware of an embedded system using real time operating system.

UNIT-I

INTRODUCTION: Embedded System-Definition, history of embedded systems, classification of embedded systems, major application areas of embedded systems, purpose of embedded systems, the typical embedded system-core of the embedded system, Memory, Sensors and Actuators, Communication Interface, Embedded firmware, Characteristics of an embedded system, Quality attributes of embedded systems, Application-specific and Domain-Specific examples of an embedded system.

UNIT-II

EMBEDDED HARDWARE DESIGN: Analog and digital electronic components, I/O types and examples, Serial communication devices, Parallel device ports, Wireless devices, Timer and counting devices, Watchdog timer, Real time clock.

UNIT-III

EMBEDDED FIRMWARE DESIGN: Embedded Firmware design approaches, Embedded Firmware development languages, ISR concept, Interrupt sources, Interrupt servicing mechanism, Multiple interrupts, DMA, Device driver programming, Concepts of C versus Embedded C and Compiler versus Cross-compiler.

UNIT-IV

REAL TIME OPERATING SYSTEM: Operating system basics, Types of operating systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling, Task communication, Task synchronization.

HARDWARE SOFTWARE CO-DESIGN: Fundamental Issues in Hardware Software Co-Design, Computational models in embedded design, Hardware software Trade-offs, Integration of Hardware and Firmware.

UNIT-V:

EMBEDDED SYSTEM DEVELOPMENT, IMPLEMENTATION AND TESTING: The integrated development environment, Types of files generated on cross-compilation, Deassembler / De-compiler, Simulators, Emulators and Debugging, Target hardware debugging,
Embedded Software development process and tools, Interpreters, Compilers and Linkers, debugging tools, Quality assurance and testing of the design, Testing on host machine, Simulators, Laboratory Tools.

Text Books:

1. Embedded Systems Architecture- By Tammy Noergaard, Elsevier Publications, 2013.
2. Embedded Systems-By Shibu. K.V-Tata McGraw Hill Education Private Limited, 2013.

References:

1. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley Publications, 2013.
2. Embedded Systems-Lyla B.Das-Pearson Publications,2013.

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Minor Course	INTERNET OF THINGS (BT24EC0M07)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Understand the new computing technologies
- Able to apply the latest computing technologies like cloud computing technology and Big Data
- Ability to introduce the concept of M2M (machine to machine) with necessary protocols
- Get the skill to program using python scripting language which is used in many IoT devices

Unit I

Introduction to Internet of Things –Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT Communication Models, Iot Communication APIs IoT enabaled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates Domain Specific IoTs – Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, Health and Lifestyle (Chap 1 and 2).

Unit II

IoT and M2M – Software defined networks, network function virtualization, difference between SDN and NFV for IoT Basics of IoT System Management with NETCOZF, YANGNETCONF, YANG, SNMP NETOPEER (Chapter 3 and 4).

Unit III

IOT Platform design Methodology, Introduction to Python - Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTPLib, URLLib, SMTPLib (Chapter 5 and 6).

Unit IV

IoT Physical Devices and Endpoints - Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input from pins., other IOT Devices (Chapter 7).

Unit V

IoT Physical Servers and Cloud Offerings – Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API, Amazon web services for IOT, Skynet IOT messaging platform (Chapter 8).

Text Books:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547.
2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD),2014, ISBN: 9789350239759.

Reference Books:

1. 1.The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence, Jan Ho¨ ller, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Aves and. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.
4. Recipes to Begin, Expand, and Enhance Your Projects, 2nd Edition, Michael Margolis, Arduino Cookbook and O'Reilly Media, 2011.

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Minor Course	DIGITAL SIGNAL PROCESSING (BT24EC0M08)	L	T	P	C
		3	0	0	3

COURSE OUTCOMES:

- Understand the concepts of discrete signals and discrete systems with its characteristics
- Calculate z-Transform, Fourier Transform, Discrete Fourier Transform of discrete signals.
- Understand the algorithms for the efficient computation of DFT coefficients of signals
- Know the various filter structures for FIR and IIR filters.
- Design the FIR and IIR filters.

Unit -I

Introduction: Signals, Systems, and Signal Processing, Classification of Signals, The Concept of Frequency in Continuous Time and Discrete Time Signals

Discrete Time Signals and Systems: Discrete Time Signals, Discrete Time Systems, Analysis of Discrete Time Linear Time Invariant Systems, Discrete Time Systems Described by Difference Equations, Implementation of Discrete Time Systems, Correlation of Discrete Time Signals

Frequency Analysis of Signals: Frequency Analysis of Continuous Time Signals, Frequency Analysis of Discrete Time Signals, Frequency Domain and Time Domain Signal Properties, Properties of the Fourier Transform for Discrete Time Signals.

Unit –II

Frequency Domain Analysis of LTI Systems: Frequency domain characteristics of LTI systems, Frequency response of LTI systems.

The z-Transform and Its Applications to the Analysis of LTI Systems: The z-Transform, Properties, Rational z Transforms, Inversion of the z-Transform, Analysis of Linear Time Invariant Systems in the z-Domain, The One sided z-Transform.

Unit –III

The Discrete Fourier Transform: Its Properties and Applications: Frequency Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT, Frequency Analysis of Signals Using DFT

Efficient Computation of the DFT: Fast Fourier Transform Algorithms: Direct Computation of the DFT, Radix-2 FFT Algorithms.

Unit –IV

Implementation of Discrete Time Systems: Structures for the Realization of Discrete Time Systems. **Structures for FIR Systems**: Direct Form Structure, Cascade Form Structures.

Structures for IIR Systems: Discrete Form Structures, Signal Flow Graphs and Transposed Structures, Cascade Form Structures, Parallel Form Structures.

Unit –V

Design of Analog Filters: Butterworth filters… Low Pass Filter, High Pass filter, Band Pass Filter, Band Reject Filter. **Design of Digital Filters**: General Considerations: Causality and Its Implications, Characteristics of Practical Frequency Selective Filters.

Design of FIR Filters: Symmetric and Antisymmetric FIR Filters, Design of Linear Phase FIR Filters Using Windows, Design of Linear Phase FIR Filters by the Frequency Sampling Method.

Design of IIR Filters From Analog Filters: IIR Filter Design by Approximation of Derivatives, IIR Filter Design by Impulse Invariance, IIR Filter Design by the Bilinear Transformation.

Frequency Transformations: Frequency Transformations in the Analog Domain, Frequency Transformations in the Digital Domain.

TEXT BOOKS:

1. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G.Manolakis, 4th Edition, Pearson Education, 2007.

Reference Books:

1. Discrete Time Signal Processing – A.V.Oppenheim and R.W. Schaffer, 3rd Edition, Pearson, 2014.
2. Digital Signal Processing-P. Ramesh Babu, 5th Edition, SCITECH Publishers.

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		L	T	P	C
Minor Course	**ELECTRONICS DEVICES AND BASIC CIRCUITS LAB (BT24EC0M12)**	**0**	**0**	**3**	**1.5**

List of Experiments:(Minimum of Ten Experiments has to be performed)

1. P-N Junction Diode Characteristics
Part A: Germanium Diode (Forward bias& Reverse bias)
Part B: Silicon Diode (Forward Bias only)
2. Zener Diode Characteristics
3. Part A: V-I Characteristics
Part B: Zener Diode as Voltage Regulator
4. Rectifiers (without)
Part A: Half-wave Rectifier
Part B: Full-wave Rectifier
5. BJT Characteristics (CE Configuration)
6. FET Characteristics (CS Configuration)
7. Transistor Biasing
8. CRO Operation and its Measurements
9. BJT-CE Amplifier
10. Emitter Follower-CC Amplifier
11. FET-CS Amplifier

Equipment required:

1. Regulated Power supplies
2. Analog/Digital Storage Oscillo scopes
3. Analog/Digital Function Generators
4. Digital Multi-meters
5. Decade Résistance Boxes/Rheostats
6. Decade Capacitance Boxes
7. Ammeters (Analogor Digital)
8. Voltmeters (Analogor Digital)
9. Active & Passive Electronic Components

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Minor Course	DIGITAL ELECTRONICS LAB (BT24EC0M13)	L	T	P	C
		0	0	3	1.5

List of Experiments: (Minimum of Ten Experiments has to be performed)

1. Verification of truth tables of Logic gates
   Two input (i) OR (ii) AND (iii) NOR (iv) NAND (v) Exclusive OR (vi) Exclusive NOR
2. Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer Kit
3. Verification of functional table of 3-to-8-line Decoder/De-multiplexer
4. four variable logic function verification using 8 to1 multiplexer.
5. Design full adder circuit and verify its functional table.
6. Verification of functional tables of
   (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) DFlip-Flop
7. Design a four bit ring counter using D Flip–Flops/JK Flip Flop and verify output
8. Design a four bit Johnson's counter using D Flip-Flops/JK Flip Flops and verify output
9. Verify the operation of 4-bit Universal Shift Register for different Modes of operation.
10. Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T- Flip-Flops and Test it with a low frequency clock and Sketch the output wave forms.
11. Design MOD–8 synchronous counter using T Flip- Flop and verify the result and Sketch the output wave forms.
12. (a) Draw the circuit diagram of a single bit comparator and test the output
    (b) Construct 7 Segment Display Circuit Using Decoder and 7 Segment LED and test it.

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Minor Course	INTERNET OF THINGS LAB (BT24EC0M14)	L	T	P	C
		0	0	3	1.5

List of Experiments: (Minimum of Twelve Experiments has to be performed)

1. Getting started with Raspberry Pi, Install Raspian on your SD card.
2. Python-based IDE(integrated development environments) for the Raspberry Pi and how to trace and debug Python code on the device.
3. Display a word on LCD, Interfacing with Raspberry Pi.
4. Using Raspberry Pi, Display Seven Segment.
5. Servo Motor Controlling with Interfacing using Raspberry Pi.
6. Soil Moisture detecting with soil moisture sensor using Raspberry Pi.
7. Calculate the distance using distance sensor Using Node MCU.
8. Basic LED functionality Using Node MCU
9. Familiarization with ARM keil MDK for programming and debugging an application on the PSoC 4 BLE chip and perform necessary software installation.
10. To interface Pushbutton/ Digital sensor(IR/LDR) with ARM keil MDKonPSoC4BLE chip and write a program to turn ONLED when push button is pressed or at sensor detection.
11. Setup a Bluetooth Low Energy (namely Bluetooth Smart) connection between the PSoC BLE kit and a smart phone and use an app to send and receive data to and from the BLE Pioneer kit.
12. To interface capacitor sensor (touch sensor) with smart phone and write a program to turn RGBLEDON/OFFwhen„1"/"0" is received from smart phone using Bluetooth.
13. Automatic street light control to control the street light (Turn on and off based on the light) using Arduino/Node MCU/Raspberry Pi
14. SmokeDetectionusingMQ-2GasSensor
15. Detecting obstacle with IR Sensor and Arduino/Node MCU/Raspberry Pi

Equipment required for Laboratories:

- Arduino/Node MCU/Raspberry Pi+PSoC4 BLE Bluetooth Low Energy Pioneer Kit + Hardware, MQ-2 Gas Sensor, Ultrasonic sound sensor.

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Minor Course	DIGITAL SIGNAL PROCESSING LAB (BT24EC0M15)	L	T	P	C
		0	0	3	1.5

(Note: Students have to perform at least FIVE experiments from each part.)

PART-A

List of the Experiments

1. Generation of DT signals.
2. Verify the Linear Convolution of two DT signals

a) Using MATLAB

b) Using Code Composer Studio (CCS)

3. Verify the Circular Convolution of two DT signals

a) Using MATLAB
b) Using Code Composer Studio (CCS)

4. Find the sum of DT sinusoidal signals.
5. Computation of Discrete Fourier Transform (DFT) and Inverse Discrete Fourier Transform (IDFT)

a) Using MATLAB
b) Using Code Composer Studio (CCS)

6. Compute N-point DFT of a given DT sequence using Decimation in Time. (Without Using Library Function)
7. Compute N-point DFT of a given DT sequence using Decimation in Frequency. (Without Using Library Function)

PART-B : Following Experiments are to be done using a TI DSP Starter Kit.

7. Generation of a sinusoidal signal.
8. Linear and circular convolution of DT sequences.
9. Compute N-point DFT of a given DT sequence
10. Design and implementation of FIR filters.
11. Design and implementation of IIR filters.

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Annexure-B

DR25
M.Tech
Regulations

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ACADEMIC REGULATIONS - DR25 FOR M. Tech (REGULAR) DEGREE COURSE

Applicable for the students admitted to M. Tech (Regular) Course from the Academic Year 2025-26 and onwards. The M. Tech Degree of Jawaharlal Nehru Technological University Kakinada shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates (i) in national level qualifying Entrance Test (GATE), (ii) AP PGECET conducted by State Government and (iii) Few Sponsored seats notified by university on the basis of any order of merit as approved by the State Government /University, subject to reservations as laid down by the Government from time to time.

2.0 AWARD OF M. Tech DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech Degree, if he pursues a course of study in not less than two and not more than four academic years. Under any circumstances, permission shall not be given to complete the course work beyond four years.

2.2 **The student shall register for all 80 credits and secure all the 80 credits.**

2.3 The minimum instruction period in each semester is 16 weeks.

3.0 PROGRAMME OF STUDY

The following specializations are offered at present for the M. Tech Programme of study.

M.Tech in

1. Computer Science & Engineering
2. Digital Electronics and Communication Systems
3. Structural Engineering
4. Machine Design

and any other course as approved by AICTE/ University from time to time.

4.0 ATTENDANCE

4.1 Attendance is calculated separately for each course. Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance in each course is 75%. A student shall not be permitted to appear for the Semester End Examinations (SEE), if his/her attendance is less than 75%.

4.2 Condoning of shortage of attendance (between 65% and 75%) up to a maximum of 10% (*considering the days of attendance in sports, games, NSS activities and medical exigencies*) in each course (Theory/Lab/Seminar) is condoned on production of valid Certificates/documents in the stipulated time mentioned here with:

4.2.1 Students who are admitted as in patients for treatment are only eligible to claim condonation of attendance. Such students under medical exigencies need to Produce (a) Doctor Medical Prescription, (ii) Medical bills duly signed by Doctor/Hospital authorities, (c) Diagnosis reports, if any, (d) Discharge summary issued at the time of discharge and any other supporting documents within two week(s) from the date of discharge to the respective institution.

Note: University at any point of time can inform the institution(s) to submit such list/proofs. *Hence, respective institution shall verify and accord condonation privilege scrupulously.*

4.2.2 Students' participation in Sports/Games and NSS activities shall also be permitted for condonation of attendance. In such cases, they need to produce (a) invitation letter from the organizing institute/agency, (ii) participation certificate and any supporting documents within two week(s) from the date of participation to the respective institution

4.3 A prescribed fee per course shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain all the relevant documents along with the request from the students, whose attendance is condoned.

4.4 Shortage of Attendance below 65% in any course shall in no case be condoned.

4.5 A Student, whose shortage of attendance is not condoned in any course(s) (Theory/Lab/Seminar) in any Semester, is considered as '**Detained in that course(s)**, and is not eligible to write Semester End Examination(s) of such Course(s), (in case of Seminar, his/her Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those course(s) in subsequent Semesters, and attend the same as and when offered.

4.6 A student shall put in a minimum required attendance in at least FOUR courses in I semester for promotion to II Semester; and at least FOUR courses in II semester for promotion to III Semester.

Re-admission / re-registration

4.7 A student shall not be permitted to appear for the Semester End Examinations (SEE) in a course unless they meet the prescribed attendance requirements for that course. Such students may take readmission for the course in the subsequent semester when it is offered by paying the prescribed fee, *at least 30 days before the commencement of classwork.* The college must obtain permission from the University by submitting the list of students eligible/applied for readmission before the commencement of classwork

4.8 Students who fail due to **less internal marks (less than 50%)** may register for the course within the maximum permissible duration of the Program.

4.9 In such a case, the candidate must re-register for the course(s) and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon eligibility for writing the end examination in those course(s).

4.10 In a semester, students are permitted to re-register maximum of THREE courses.

4.11 Upon re-registration, the student's previous performance in the respective course(s) will be nullified. Re-registration must be completed by paying the prescribed fee at least 30 days prior to the commencement of classwork. The college is required to obtain approval from the University by submitting a list of eligible and interested students before the start of commencement of classwork.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory courses 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The continuous / internal evaluation shall be made based on the **average** of the marks secured in the two CIE/Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each CIE/midterm examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks. End semester examination is conducted for 60 marks for all FIVE (5) questions (one question from one unit) to be answered (either or).

5.2 For practical courses, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks. The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with breakup marks of Procedure-**15,** Experimentation- **25,** Results-10, Viva-voce-10.

5.3 For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher of the respective college and the second examiner shall be appointed by the University from the panel of examiners submitted by the respective college.

5.8 Students shall undergo mandatory summer internship / industrial training (3 credits) for a minimum of **eight weeks duration** at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before the committee. The Committee comprises of a HoD / Professor of the department and two faculty. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.9 The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. The examination committee will be constituted by the HoD and Professor of the department and two faculty. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.0 EVALUATION OF SEMINAR/INTERNSHIP/DISSERTATION WORK

All the students admitted under these regulations have to mandatorily comply the requirements of (i) Seminar-I, (ii) Seminar-II, (iii) Comprehensive Viva, (iv) Dissertation Part-A and (v) Dissertation Part-B. Out of these, (i) to (iv) are evaluated by internally by Project Review Committee (PRC) and (v) External Evaluation.

6.1 A Project Review Committee (PRC) shall be constituted with Head of the Department and Two other senior faculty members in the department.

6.2 Students are required to appear for Seminar-I and Seminar-II in First and Second semester respectively. They shall present before PRC on the topic of their choice/interest preferably on the courses listed in respective semesters. PRC shall advise the students in advance to select topics which strengthen their Dissertation Part-A and Dissertation Part-B.

6.3 Students shall undergo mandatory summer internship / industrial training (*2 credits*) for a minimum of eight weeks duration at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before PRC. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.4 The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.5 Registration of Dissertation/Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical and duly approved by PRC.

6.6 After satisfying 6.5, student has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval

6.7 If a candidate wishes to change his/her supervisor or topic of the project, he/she can do so with the approval of PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.8 Continuous assessment of Dissertation-Part A and Dissertation-Part B during the Semester(s) will be monitored by PRC. *Dissertation-Part A* will be only internal evaluation by PRC for 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.9 The candidate shall submit a status report to the PRC in two stages, each accompanied by an oral presentation, with a minimum interval of three months between the two.

6.10 The work on the project shall be initiated at the beginning of the III Sem and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis *(Dissertation – Part A & Part B)* only with the approval of PRC not earlier than 40 weeks from the date of registration of the project work.

6.11 Three copies of the project thesis, printed on both sides of the page and certified by the supervisor, shall be submitted to the College/Institute along with the plagiarism report.

6.10 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.11 If the report of the examiner is *not favourable*, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is *not favourable* again, the thesis shall be summarily rejected. The

candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University.

6.12 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination. The Board shall jointly report the candidate's work for a maximum of 100 marks. Corresponding grade will be awarded by the University.

6.13 If the report of the Viva-Voce is unsatisfactory (i.e., < 50 marks), the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.

7.0 Cumulative Grade Point Average (CGPA)

Marks Range (Max – 100)	Letter Grade	Level	Grade Point
≥ 90	S	Outstanding	10
≥80 to <90	A	Excellent	9
≥70 to <80	B	Very Good	8
≥60 to <70	C	Good	7
≥50 to <60	D	Fair	6
<50	F	Fail	3
		Absent	0

Computation of SGPA

- The following procedure is to be adopted to compute the Semester Grade Point Average(SGPA) and Cumulative Grade Point Average (CGPA):
- The **SGPA** is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e
  SGPA (Si) = $\sum$ (Ci X Gi) / $\sum$ Ci
- Where Ci is the number of credits of the i^{th} course and Gi is the grade point scored by the student in the i^{th} course.

Computation of CGPA

- The **CGPA** is also calculated in the same manner taking into account all the courses undergone by a student over all the semester of a Programme, i.e.
  CGPA = $\sum$ (Ci X Si) / $\sum$ Ci
- Where Si is the SGPA of the i^{th} semester and Ci is the total number of credits in that semester.
- The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
- Equivalent Percentage = (CGPA- 0.5) x 10

8.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	CGPA to be secured	
First Division with Distinction	≥ 7.5 (without supplementary History)	From the CGPA secured from 80 credits
First Class	≥ 6.5	
Second Class	≥ 6.0 to < 6.5	

The secured grade, grade points, status and credits obtained will be shown separately in the memorandum of marks. If a student wants to leave the program / exit after successful completion of first two semesters, he/she will be awarded Post Graduate Diploma in the specialization concerned.

9.0 WITHHOLDING OF RESULTS

If the student is involved in indiscipline/malpractices/court cases, the result of the student will be withheld.

10.0 GENERAL

10.1 Wherever the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

10.4 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

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MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	Both the candidates involved in the malpractice will forefeit their seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.

12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators:

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

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Programme Structure

R25 M.Tech Course Structure

M.Tech (XXXX) I – Semester

S. No.	Course Code	Course Title	L	T	P	C
1		Program Core – 1	3	1	0	4
2		Program Core – 2	3	1	0	4
3		Program Core – 3	3	1	0	4
4		Program Elective – I	3	0	0	3
5		Program Elective – II	3	0	0	3
6		Laboratory – 1	0	1	2	2
7		Laboratory – 2	0	1	2	2
8		Seminar-I	0	0	2	1
		TOTAL	**15**	**5**	**6**	**23**

List of Professional Elective Courses in I Semester (Electives – I & II)

S.No.	Course Code	Course Title
1		
2		
3		
4		
5		
6		
7		
8		

@ Minimum 2/3 themes per elective

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M.Tech (XXXX) II – Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1		Program Core – 4	3	1	0	4
2		Program Core – 5	3	1	0	4
3		Program Core – 6	3	1	0	4
4		Program Elective – III	3	0	0	3
5		Program Elective - IV	3	0	0	3
6		Laboratory – 3	0	1	2	2
7		Laboratory – 4	0	1	2	2
8		Seminar – II	0	0	2	1
		TOTAL	**15**	**5**	**6**	**23**

List of Professional Elective Courses in II Semester (Electives III & IV)

S.No.	Course Code	Course Title
1		
2		
3		
4		
5		
6		
7		
8		

@ Minimum 2/3 themes per elective

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M.Tech (XXXX) - III Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1		Research Methodology and IPR / *Swayam 12 week MOOC course – RM&IPR*	3	0	0	3
2		Summer Internship/ Industrial Training (8-10 weeks)*	-	-	-	3
3		Comprehensive Viva#	-	-	-	2
4		Dissertation Part – A$	-	-	20	10
		TOTAL	**3**	**-**	**20**	**18**

* Student attended during summer / year break and assessment will be done in 3rd Sem.
# Comprehensive viva can be conducted courses completed upto second sem.
$ Dissertation – Part A, internal assessment

M.Tech (XXXX) – IV Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1		Dissertation Part – B%	-	-	32	16
		TOTAL	**-**	**-**	**32**	**16**

% External Assessment

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Revised Bloom's Taxonomy Action Verbs

Definitions	I. Remembering	II. Understanding	III. Applying	IV. Analyzing	V. Evaluating	VI. Creating
Bloom's Definition	Exhibit memory of previously learned material by recalling facts, terms, basic concepts, and answers.	Demonstrate understanding of facts and ideas by organizing, comparing, translating, interpreting, giving descriptions, and stating main ideas.	Solve problems to new situations by applying acquired knowledge, facts, techniques and rules in a different way.	Examine and break information into parts by identifying motives or causes. Make inferences and find evidence to support generalizations.	Present and defend opinions by making judgments about information, validity of ideas, or quality of work based on a set of criteria.	Compile information together in a different way by combining elements in a new pattern or proposing alternative solutions.
Verbs	• Choose • Define • Find • How • Label • List • Match • Name • Omit • Recall • Relate • Select • Show • Spell • Tell • What • When • Where • Which • Who • Why	• Classify • Compare • Contrast • Demonstrate • Explain • Extend • Illustrate • Infer • Interpret • Outline • Relate • Rephrase • Show • Summarize • Translate	• Apply • Build • Choose • Construct • Develop • Experiment with • Identify • Interview • Make use of • Model • Organize • Plan • Select • Solve • Utilize	• Analyze • Assume • Categorize • Classify • Compare • Conclusion • Contrast • Discover • Dissect • Distinguish • Divide • Examine • Function • Inference • Inspect • List • Motive • Relationships • Simplify • Survey • Take part in • Test for • Theme	• Agree • Appraise • Assess • Award • Choose • Compare • Conclude • Criteria • Criticize • Decide • Deduct • Defend • Determine • Disprove • Estimate • Evaluate • Explain • Importance • Influence • Interpret • Judge • Justify • Mark • Measure • Opinion • Perceive • Prioritize • Prove • Rate • Recommend • Rule on • Select • Support • Value	• Adapt • Build • Change • Choose • Combine • Compile • Compose • Construct • Create • Delete • Design • Develop • Discuss • Elaborate • Estimate • Formulate • Happen • Imagine • Improve • Invent • Make up • Maximize • Minimize • Modify • Original • Originate • Plan • Predict • Propose • Solution • Solve • Suppose • Test • Theory

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DR25
M.Tech
Course Structure
&
Syllabus

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DR25-COURSE STRUCTURE & SYLLABUS
for
M. Tech -ECE

Digital Electronics & Communication Systems (DECS) Programme

(Applicable for batches admitted from 2025-2026)

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I Year-I Semester

S. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	D2513800	Mathematical Foundation for Communication Engineering	3	1	0	4
2.	D2513801	Digital System Design	3	1	0	4
3.	D2513802	Wireless Communications & Networks	3	1	0	4
4.	D25138A0 D25138A1 D25138A2	**Elective I** 1. Software Defined Radio 2. Optical Communication & Networks 3. Radio and Navigational Aids	3	0	0	3
5.	D25138B0 D25138B1 D25138B2	**Elective II** 1. FPGA and ASIC Design 2. System Design with RTOS & Embedded LINUX 3. System Design Using Verilog	3	0	0	3
6.	D2513803	Digital System Design Laboratory	0	1	2	2
7.	D2513804	Wireless Communications Laboratory	0	1	2	2
8.	D2513805	Seminar – 1	0	0	2	1
Total Credits			**15**	**5**	**6**	**23**

List of Professionals Elective Courses in I Semester (Electives-I & II)

S. No.	Course Title	Course Code
1	Software Defined Radio	D25138A0
2	Optical Communication & Networks	D25138A1
3	Radio and Navigational Aids	D25138A2
4	FPGA and ASIC Design	D25138B0
5	System Design with RTOS and Embedded LINUX	D25138B1
6	System Design Using Verilog	D25138B2

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I Year-II Semester

S. No.	Course Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1.	D3823800	Information Theory and Coding	3	1	0	4
2.	D3823801	IoT & its Communication Protocols	3	1	0	4
3.	D2523802	Embedded System Design	3	1	0	4
4.	D25238A0 D25238A1 D25238A2	**Elective III** 1. Design for Testability 2. MEMS 3. System on Chip Design	3	0	0	3
5.	D25238B0 D25238B1 D25238B2	**Elective IV** 1. Detection and Estimation Theory 2. EMI/ EMC 3. ARM Controllers and Embedded C	3	0	0	3
6.	D2523803	Internet of Things Lab	0	1	2	2
7.	D2523804	Embedded System Design Lab	0	1	2	2
8.	D2523805	Seminar – 2	0	0	2	1
Total Credits			**15**	**5**	**6**	**23**

List of Professionals Elective Courses in II Semester (Electives- III & IV)

S. No	Course Title	Course Code
1	Design for Testability	D25238A0
2	MEMS	D25238A1
3	System on Chip Design	D25238A2
4	Detection and Estimation Theory	D25238B0
5	EMI/ EMC	D25238B1
6	ARM Controllers and Embedded C	D25238B2

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II Year-III Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	D2530000	Research Methodology and IPR/ Swayam 12-week MOOC course – RM & IPR	3	0	0	3
2	D2533801	Summer Internship / Industrial Training (8-10 weeks) *	-	-	-	3
3	D2533802	Comprehensive Viva#	-	-	-	2
4	D2533803	Dissertation Part – A$	0	0	20	10
Total			**3**	**0**	**20**	**18**

*Student attended during summer / year break and assessment will be done in 3rd sem.
Comprehensive viva can be conducted courses completed up to second sem.
$ Dissertation – Part A, internal assessment

II Year-IV Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	D2543800	Dissertation Part – B%	--	--	32	16
	Total Credits		--	--	32	**16**

% External Assessment

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I Semester	MATHEMATICAL FOUNDATION FOR COMMUNICATION ENGINEERING (D2513800)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. Understand foundational concepts of probability, sampling distributions, estimation, and hypothesis testing for statistical data analysis.
2. Develop analytical skills to handle random processes and Markov chains essential in stochastic modelling and simulation.
3. Acquire computational techniques for solving numerical problems involving interpolation, root finding, ODEs, and eigenvalue problems.
4. Explore mathematical optimization through multivariable calculus, constrained optimization techniques, and numerical methods.
5. Introduce wavelet transform concepts and their application to multi-resolution analysis in data and signal processing.

UNIT- I: Probability and Statistics:

Sampling distributions, Estimation of parameters (point estimation – unbiasedness & minimum variance, basics of interval estimation – confidence interval for mean), Testing of hypotheses (one and two sample tests for mean), Linear regression, Introduction to non-linear regression.

UNIT - II: Stochastic process:

Random processes, Random Walk, Markov process with special emphasis on Markov chain.

UNIT-III: Numerical Analysis:

Introduction to Interpolation formulae [Bessel's & Sterling's], Roots of transcendental equations [Bisection, Regula-Falsi & Newton-Raphson] Solutions of simultaneous non-linear equations [Newton's method], Numerical solution of Ordinary Differential equation [Modified Euler's method, fourth order Runga - Kutta method], Matrix Eigen value and Eigen vector problems.

UNIT- IV: Optimization Technique:

Calculus of several variables, Implicit function theorem, Nature of singular points, Necessary and sufficient conditions for optimization, Constrained Optimization, Lagrange multipliers, Gradient method – steepest descent method.

UNIT- V: Wavelet Transform:

Resolution problems, Multi-resolution analysis, Continuous & discrete wavelet transform

TEXT BOOKS:

1. A. Papoulis and S. Unnikrishnan Pillai, ``Probability, Random Variables and Stochastic Processes," Fourth Edition, McGraw Hill. (Indian Edition is available).
2. Gibert Strang," Linear Algebra and its applications", Thomson Learning Inc, 4th Edition.

REFERENCE BOOKS:

1. H. Stark and J. Woods, 'Probability and Random Processes with Applications to Signal Processing," Third Edition, Pearson Education. (Indian Edition is available).
2. Steven M. Kay, " Intuitive Probability and Random Process using MATLAB", Springer Publications.
3. To dd K Moon, Wynn C. Stirling" Mathematical Methods and Algorithms for Signal Processing, Prentice Hall.

COURSE OUTCOMES

By the end of this course, students will be able to:

1. Apply statistical methods including point estimation, confidence intervals, and hypothesis testing to real-world data scenarios.
2. Model and analyse stochastic systems using random processes, random walks, and Markov chains.
3. Solve engineering and scientific problems using numerical techniques such as Newton-Raphson, interpolation methods, and Runge-Kutta for differential equations.
4. Perform optimization tasks with or without constraints using gradient-based techniques and understand the role of Lagrange multipliers.
5. Use wavelet transforms to analyse signals and data with applications in compression and resolution enhancement.

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I Semester	DIGITAL SYSTEM DESIGN (D2513801)	L	T	P	C
		3	1	0	4

Course Objectives:

1. Designing digital circuits, behavior and RTL modelling of digital circuits using Verilog HDL, verifying these Models and synthesizing RTL models to standard cell libraries and FPGAS.
2. Students gain practical experience by designing, modelling, implementing and verifying several digital
3. This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools

UNIT - I:

Introduction to Veril Log HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II:

Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

UNIT -III:

Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators, Design at dataflow level, Parameter and constant usage in dataflow.

UNIT - IV:

Behavioral Modelling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioral Level

UNIT -V:

Verilog Procedural and Control Constructs: Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

TEXTBOOKS:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. Zainalabdien Navabi, Verliog Digital System Design, TMH, 2nd Edition.

REFERENCE BOOKS:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL -Michel D. Ciletti, PHI,2009.

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Understand the syntax, semantics, and simulation principles of Verilog HDL for digital system modelling.
2. Design and implement digital circuits using gate-level modelling and primitive components.
3. Develop dataflow-level models for digital systems using continuous assignments and operators.
4. Apply behavioral modelling techniques to describe complex digital systems using procedural constructs.
5. Utilize control constructs in Verilog to simulate, test, and verify digital designs effectively.

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I Semester	WIRELESS COMMUNICATIONS & NETWORKS (D2513802)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. To introduce the cellular system design concepts including frequency reuse, interference management, and handoff strategies.
2. To understand large-scale radio wave propagation models and their impact on wireless system performance.
3. To study small-scale fading, multipath propagation effects, and statistical models for channel behavior.
4. To explore equalization and diversity techniques for improving signal quality in wireless environments.
5. To provide an overview of wireless networks and standards such as IEEE 802.11, IEEE 802.16, and wireless PANs.

UNIT-I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Trunking and Grade of Service.

UNIT-II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, Basic Propagation Mechanisms, **Reflection**: Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, **Diffraction**: Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife- edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT -III

Mobile Radio Propagation: Small–Scale Fading and Multipath Small Scale Multipath propagation- Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT-IV

Equalization and Diversity Introduction, Fundamentals of Equalization, Training a Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non-linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity -Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization
Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT-V

Wireless Networks Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11, IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – GottapuSasi bhushanaRao, Pearson Education, 2012.

REFERENCE BOOKS:

1. Principles of Wireless Networks – KavehPahLaven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – KamiloFeher, 1999, PHI. Wireless Communication and Networking – William Stalling

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Understand cellular system design concepts including frequency reuse, interference management, and handoff strategies.
2. Analyse large-scale radio propagation models and apply them to outdoor and indoor wireless environments.
3. Evaluate small-scale fading effects and multipath propagation using statistical and empirical models.
4. Apply equalization and diversity techniques to improve wireless communication performance under varying channel conditions.
5. Demonstrate knowledge of wireless network standards, architectures, and protocols including IEEE 802.11 and 802.16.

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I Semester	SOFTWARE DEFINED RADIO (D25138A0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Introduce the evolution of radio communication systems and the fundamental concepts, architectures, and design principles of Software Defined Radio (SDR).
2. Understand the implementation challenges in RF front-end systems, including dynamic range, receiver topologies, and performance-affecting factors.
3. Explore digital signal generation techniques, particularly direct digital synthesis (DDS), and analyse related spurious signal behaviors.
4. Introduce multirate signal processing methods such as sample rate conversion, polyphase filters, and timing recovery in digital receivers.
5. Study analog-to-digital and digital-to-analog conversion techniques and methods for improving data converter performance in SDR systems.

UNIT- I:

Introduction to Software radio concepts: Introduction, need, characteristics, benefits and design principles of Software Radios. Traditional radio implemented in hardware (first generations of 2G cell phones), Software controlled radio (SCR), Software defined radio (SDR), Ideal software radio (ISR), Ultimate software radio (USR)

UNIT- II:

Radio frequency implementation issues: The purpose of RF Front-End, Dynamic range, RF Receiver Front-End Topologies, Enhanced Flexibility of the RF Chain with Software Radios, Importance of Components to Overall performance, Transmitter Architecture and their issues, Noise and Distortion in RF Chain.

UNIT -III:

Digital generation of signals: Introduction, Comparison of Direct Digital Synthesis with Analog Signal Synthesis, Approaches to Direct Digital Synthesis, Analysis of Spurious Signals, Spurious components due to Periodic Jitter.

UNIT-IV:

Multirate Signal Processing: Introduction, Sample Rate Conversion Principles, Polyphase Filters, Digital Filter Banks, Timing Recovery in Digital receivers Using Multirate Digital Filters.

UNIT- V:

A/D & D/A Conversion: Introduction, Parameters of Ideal Data Converters, Parameters of Practical data Converters, Techniques to improve Data Converter performance, JTRS.

TEXT BOOKS:

1. Jeffery H. Reed, "Software Radio, (A modern approach to radio engineering)", PHI PTR, 2002
2. John J. Rouphael, "RF and Digital Signal Processing for Software Defined Radio" Elsevier, Newness Publications.

REFERENCE BOOKS:

1. C. Richard Johnson, Jr., and William A. Sethares, Telecommunication Breakdown, Prentice Hall, ISBN 0-13-143047-5, 2004
2. Software Defined Radio: Theory and Practice by John M. Reyland (Artech House, 2023)

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Know the fundamentals of Software Radios, their evolution from traditional radios, and various levels including SCR, SDR, ISR, and USR.
2. Analyse RF front-end architectures, dynamic range requirements, and the role of RF Components in system performance for Software Radio implementation.
3. Explain and compare different signal generation techniques including direct digital synthesis, and analyse sources of spurious components and jitter effects.
4. Apply multi-rate signal processing techniques such as sample rate conversion, polyphase Filtering, and digital filter banks in software radio systems.
5. Evaluate the performance of A/D and D/A converters in practical systems, and describe Methods to improve conversion performance, including relevance to JTRS

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I Semester	OPTICAL COMMUNICATION & NETWORKS (D25138A1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Introduce the fundamentals of optical fiber communication, including transmission link components, light propagation, and fiber structures.
2. Understand the principles and performance of optical sources and detectors used in optical communication systems.
3. Explain the structure and function of optical communication systems, including digital systems and modern high-speed links.
4. Familiarize students with components and technologies used in fiber optic networks and their architectures.
5. Explore coherent communication systems, detection techniques, and the role of demodulation and noise management in optical receivers.

UNIT- I:

Overview of optical fiber communications: Elements of an optical fiber transmission link. Optical Fibers: structures, wave guiding, Nature of light, Basic optical laws and definitions, optical fiber modes and configurations (Fiber types, Rays and modes, step index and graded index fibers) mode theory of circular waveguides. (Qualitative Treatment) Fabrication, cabling and installation: Fabrication, fiber optic cables, Installation- placing the cable.

UNIT -II:

Optical sources: LEDs, structures, quantum efficiency, modulation capability, Laser diodes: Laser diodes and threshold conditions, external quantum efficiency resonant frequencies, **Optical Detectors**: Physical principles of photodiodes (pin Photodiode, avalanche, photo diode) comparison of photo detectors, noise in detectors.

UNIT -III:

Optical Communication Systems: Block diagrams of optical communication systems, direct intensity modulation, digital communication systems, Laser semiconductor transmitter, Generations of optical fiber link, description of 8 Mb/s optical fiber communication link, description of 2.5 Gb/s optical fiber communication link.

UNIT -IV:

Components of fiber optic Networks: Overview of fiber optic networks, Trans receiver, semiconductors optical amplifiers, couplers/splicer's, wavelength division multiplexers and demultiplexers, filters, isolators and optical switches. **Fiber Optic Networks**: Basic networks, SONET/SDIT, Broad cast and select WDM Networks, wavelength routed networks, optical CDMA Nonlinear effects on network performance.

UNIT- V:

Coherent Systems: Coherent receiver, Homodyne and heterodyne detection, noise in coherent receiver, polarization control, Homodyne receiver, Reusability and laser line-width, heterodyne receiver, synchronous, Asynchronous and self-synchronous demodulation, phase diversity receivers.

TEXT BOOKS:

1. Optical fiber communications – Gerd Keiser, 3 rd Ed. MGH.
2. Fiber Optic Communication Technology – Djafar K. Mynbaev and Lowell L. Scheiner,
3. Optoelectronic devices and systems – S.C. Gupta, PHI, 2005.

REFERENCE BOOKS:

1. Fiber Optics Communications – Harold Kolimbiris (Pearson Education Asia)
2. Optical Fiber Communications and its applications – S.C. Gupta (PHI) 2004.

COURSE OUTCOMES:

Upon completion of the course students will be able to :

1. Explain the fundamental principles of optical fiber communication including Wave guiding, fiber types, and mode theory of circular waveguides.
2. Compare and analyze various optical sources (LEDs, laser diodes) and detectors (PIN, APD) in terms of efficiency, modulation capability, and noise performance.
3. Design and interpret the block diagrams of optical communication systems and explain the working of digital systems including 8 Mb/s and 2.5 Gb/s optical links.
4. Evaluate different fiber optic network components such as transceivers, amplifiers, WDM Systems.
5. Demonstrate understanding of coherent optical systems including homodyne/heterodyne detection, polarization effects, and noise handling in coherent receivers.

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I Semester	RADIO AND NAVIGATIONAL AIDS (D25138A2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Understand the principles and configurations of radio positioning systems and factors affecting positioning accuracy.
2. Explore terrestrial radio navigation systems including LORAN, ILS, and indoor/urban positioning technologies.
3. Introduce fundamental navigation concepts such as position fixing, dead reckoning, and integrated navigation systems.
4. Study advanced satellite navigation techniques including Differential GNSS and carrier-phase positioning.
5. Examine inertial navigation systems and their equations, alignment methods, and error propagation models.

UNIT- I: Principles of Radio Positioning: Radio Positioning Configurations and Methods, Positioning Signals, User Equipment, Propagation, Error Sources, and Positioning Accuracy. Terrestrial Radio Navigation: Point-Source Systems, Loran, Instrument Landing System, Urban and Indoor Positioning, Relative Navigation, Tracking, Sonar Transponders.

UNIT- II: Introduction to Navigation: What Is Navigation, Position Fixing, Dead Reckoning, Inertial Navigation, Radio and Satellite Navigation, Terrestrial Radio Navigation, Satellite Navigation, Feature Matching, The Complete Navigation System.

UNIT- III: Advanced Satellite Navigation: Differential GNSS, Carrier-Phase Positioning and Attitude, Poor Signal-to-Noise Environments, Multipath Mitigation, Signal Monitoring, Semi Codeless Tracking.

UNIT- IV: Inertial Navigation: Inertial-Frame Navigation Equations, Earth-Frame Navigation Equations, Local-Navigation-Frame Navigation Equations, Navigation Equations Precision, Initialization and Alignment, INS Error Propagation, Platform INS, Horizontal-Plane Inertial Navigation.

UNIT- V: Satellite Navigation & GNSS Systems: Fundamentals: GPS, GLONASS, Galileo, Beidou, IRNSS, signal structure, measurement errors (ionospheric/tropospheric/multipath), Dilution of Precision (GDOP, PDOP), ephemeris, clock/correction errors, Differential GNSS, WAAS, integrity monitoring, carrier-phase techniques.

TEXT BOOKS:

1. G S RAO, Global Navigation Satellite Systems, McGraw-Hill Publications, New Delhi, 2010.
2. Principles of GNSS, Inertial, and Multisensor Integrated Navigation Systems, Paul D. Groves Artech House, 2008 and 2013 Second Edition.
3. 2. B. Hofmann Wollenhof, H. Lichtenegger, and J. Collins, "GPS Theory and Practice", Springer Wien, New York, 2000.

REFERENCE BOOKS:

1. Pratap Misra and Per Enge, "Global Positioning System Signals, Measurements, and Performance," Ganga-Jamuna Press, Massachusetts, 2001.
2. Ahmed El-Rabbany, "Introduction to GPS," Artech House, Boston, 2002.
3. Bradford W. Parkinson and James J. Spilker, "Global Positioning System: Theory and Applications," Volume II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Explain the principles, configurations, and error sources of terrestrial and radio positioning systems.
2. Apply various navigation methods to determine position and trajectory.
3. Analyse advanced satellite navigation techniques for accuracy enhancement.
4. Evaluate inertial navigation equations, alignment methods, and error propagation.
5. Integrate GNSS systems with error correction techniques for reliable navigation solutions.

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I Semester	FPGA and ASIC DESIGN (D25138B0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the evolution, design flow, and applications of FPGAs and PLDs.
2. To study various FPGA/CPLD programming technologies and commercially available devices.
3. To understand the internal architecture and building blocks of FPGAs/CPLDs and their impact on performance.
4. To explore routing architectures and strategies used in different FPGA types.
5. To analyse architectural elements and apply FPGA technology in real-world case studies.

UNIT-I:

INTRODUCTION TO FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.

DESIGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter

UNIT-II:

FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Axtel's FPGA, Altera's FPGA/CPLD.

UNIT-III:

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT-IV:

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures

UNIT-V:

FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA CASE STUDY – Applications using Kintex-7, Virtex-7, Artix-7.

TEXT BOOKS:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
2. VLSI Design: A Practical Guide for FPGA and ASIC Implementations by Vikram A. Chandrasetty (Springer Briefs, 2011).

REFERENCE BOOKS:

1. Data sheets of Artix-7, Kintex-7, Virtex-7
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

COURSE OUTCOMES:

Upon completion of the course students will be able to :

1. Explain the evolution, design flow, and practical applications of FPGAs and PLDs.
2. Compare different FPGA/CPLD devices and their programming technologies.
3. Analyse the architecture of logic blocks, routing structures, and I/O blocks in FPGAs.
4. Apply routing techniques to various FPGA architectures for optimized performance.
5. Demonstrate FPGA design implementation using case studies on Kintex-7, Virtex-7, and Artix-7.

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I Semester	SYSTEM DESIGN WITH RTOS & EMBEDDED LINUX (D25138B1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the key concepts of Real-Time Operating Systems and task management fundamentals.
2. To explore synchronization and communication mechanisms used in real-time systems.
3. To understand the role of exceptions, interrupts, and timer services in RTOS environments.
4. To provide hands-on experience with Linux kernels and shell scripting for embedded applications.
5. To analyse embedded Linux architecture and understand the process of application porting and driver integration.

UNIT- I: Introduction to RTOS and Task Management

Introduction to Real-Time Operating Systems (RTOS): Key characteristics, scheduler, kernel objects and services, system calls, static and dynamic libraries, cross tool chains, Task management: Defining tasks, task states, scheduling, task operations, synchronization, communication, concurrency.

UNIT- II: Synchronization, Communication, and I/O Systems

Semaphores: Operations, use cases, Message Queues: Types, operations, use cases (including pipes, event registers, signals, condition variables), I/O Subsystems: I/O concepts, subsystems, Synchronization and Communication: Resource synchronization methods, critical section, design patterns, priority inversion, common design problems (deadlocks, priority inversion).

UNIT- III: Exceptions, Interrupts, and Timer Services

Exceptions and Interrupts: Definitions, applications, spurious interrupts, Timer Services: Real-time clocks, system clocks, programmable interval timers, timer interrupt service routines.

UNIT -IV: Linux Kernel and Shell Scripting

Introduction to Linux Kernels: Linux basics, GNU utilities, distributions, access methods (CLI, graphical terminal emulators), Bash Shell Commands: Navigation, file handling, system monitoring, environment variables, user-defined variables, Shell Scripting: Script creation, control structures (if-else, loops, case commands), output redirection, practical examples, handling signals, background scripts, basic script functions, alternative shells (dash, zsh).

UNIT -V: Embedded Linux Architecture and Application Porting

Embedded Linux Architecture: Kernel architecture, memory manager, scheduler, file system, I/O and networking subsystems, IPC, user space, startup sequence, Board Support Package: Embedded storage (MTD), embedded file system, embedded device drivers (communication kernel modules), Porting Applications: Real-time Linux, hard real-time programming, building and debugging (bootloaders, kernel, root file system, device tree).

TEXT BOOKS:

1. Qing Li, Caroline Yao (2020), "Real-Time Concepts for Embedded Systems", CMP Books.

2. Chris Simmonds, "Mastering Embedded Linux Programming" - Second Edition, PACKT Publications Limited.

REFERENCE BOOKS:

1. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates.

2. Mastering Embedded Linux Programming (3rd Edition) by Frank Vasquez & Chris Simmonds.

COURSE OUTCOMES:

After completing the course, students will be able to:

1. Describe RTOS features, kernel components, and manage task scheduling and synchronization.
2. Implement inter-task communication using semaphores, message queues, and handle I/O operations effectively.
3. Analyse the behaviour of exceptions, interrupts, and use timer services in real-time systems.
4. Use Linux shell commands and scripts to perform system-level operations and automation tasks.
5. Demonstrate understanding of embedded Linux internals and port applications with BSP and device drivers.

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I Semester	SYSTEMS DESIGN USING VERILOG (D25138B2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. Designing digital circuits, behaviour and RTL modelling of digital circuits using verilog HDL, verifying these Models and synthesizing RTL models to standard cell libraries and FPGAS.
2. Students gain practical experience by designing, modelling, implementing and verifying several digital
3. This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools.

UNIT - I: Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II: Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

UNIT -III: Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators, Design at dataflow level, Parameter and constant usage in dataflow.

UNIT - IV: Behavioural Modelling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioural Level

UNIT -V: Verilog Procedural and Control Constructs: Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

TEXT BOOKS:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. Zainalabdien Navabi, Verliog Digital System Design, TMH, 2nd Edition.

REFERENCE BOOKS:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL -Michel D. Ciletti, PHI,2009.

COURSE OUTCOMES:

Upon completion of the course students will be able to:

1. Describe Verilog hardware description, languages (HDL).
2. Design digital circuits.
3. Write Behavioral models of digital circuits.
4. Write Register Transfer Level (RTL) models of Digital Circuits.
5. Verify Behavioral and RTL models.

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I Semester	DIGITAL SYSTEM DESIGN LABORATORY (D2513803)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To introduce algorithms for efficient combinational and sequential logic design such as CAMP-I, CAMP-II, and Kohavi.
2. To familiarize students with programmable logic array (PLA) design, minimization, and folding techniques.
3. To develop skills in the design and implementation of ROM and control logic units.
4. To enable practical experience in digital system implementation using FPGA platforms.
5. To understand and experiment with error detection/correction and finite state machine design concepts.

Systems Design experiments:

- The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
- Consider the suitable switching function and data to implement the required logic if required.

A student must do at least 10 Experiments.

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm)
5. PLA folding algorithm (COMPACT algorithm)
6. ROM design.
7. Control unit and data processor logic design
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Apply CAMP-I and CAMP-II algorithms to determine essential, secondary, and spurious prime implicants.
2. Implement PLA minimization and folding using IISc and COMPACT algorithms respectively.
3. Design **and** realize ROM-based systems and control/data path logic circuits.
4. Develop digital systems using FPGA tools and platforms for real-time applications.
5. Perform logic minimization using Kohavi's algorithm and **analyze** error-correcting codes through Hamming experiments.

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I Semester	WIRELESS COMMUNICATIONS LABORATORY (D2513804)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To understand and analyse digital communication techniques including error detection and correction.
2. To provide hands-on experience in spread spectrum systems, convolutional coding, and decoding.
3. To apply signal processing techniques using transforms, filtering, and DSP hardware platforms.
4. To explore image processing operations and study their effects on digital images.
5. To study and experiment with optical fiber communication, mobile phone trainers, CDMA, and ISDN systems.

PART A: List of Experiments :(Minimum of Ten Experiments must be performed)

1. Measurement of Bit Error Rate using Binary Data.
2. Verification of minimum distance in Hamming code
3. Determination of output of Convolution Encoder for a given sequence.
4. Determination of output of Convolution Decoder for a given sequence.
5. Efficiency of DS Spread- Spectrum Technique
6. Simulation of Frequency Hopping (FH) system
7. Effect of Sampling and Quantization of Digital Image
8. Verification of Various Transforms (FT / DCT/ Walsh / Hadamard) on a given Image (Finding Transform and Inverse Transform)
9. Point, Line and Edge detection techniques using derivative operators.
10. Implementation of FIR filter using DSP Trainer Kit (C-Code/ Assembly code)
11. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code).
12. Determination of Losses in Optical Fiber.
13. Observing the Waveforms at various test points of a mobile phone using Mobile Phone Trainer.
14. Study of Direct Sequence Spread Spectrum Modulation & Demodulation using CDMA-DSSBER Trainer.
15. Study of ISDN Training System with Protocol Analyzer.
16. Characteristics of LASER Diode.

PART B: Equipment required for Laboratory Software:

1. MATLAB along with Simulink Licensed simulation software tool with communication and Signal processing Toolbox.
2. Computer Systems with required specifications

Hardware:

1. Hardware kits for verification of BER
2. Hardware kits of Convolution encoders, Hamming encoders.
3. Frequency spectrum
4. Mobile Phone Trainer
5. DSP Trainer Kit
6. CDMA-DSS-BER Trainer
7. ISDN Training System with Protocol Analyzer
8. Optical fiber Transmitter and receiver kit along with different lengths of cables

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Measure bit error rates and verify error correction capabilities using Hamming codes.
2. Simulate and analyse convolutional encoder/decoder systems and spread spectrum techniques.
3. Implement and evaluate digital signal processing algorithms (FIR/IIR filters) on DSP trainer kits.
4. Apply transforms (FT, DCT, Walsh, Hadamard) and perform edge/line detection in digital images.
5. Experiment with optical fiber characteristics, mobile phone trainer systems, and CDMA/ISDN technologies.

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I Semester	SEMINAR – I (D2513805)	L	T	P	C
		0	0	2	1

For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

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II Semester	INFORMATION THEORY AND CODING (D2523800)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. Introduce core concepts of information theory including entropy and mutual information.
2. Teach lossless source coding algorithms like Huffman, Arithmetic, and LZW.
3. Explain channel capacity and its evaluation for various communication channels.
4. Explore the fundamentals of video and speech coding techniques.
5. Provide knowledge of error control coding for reliable data transmission.

UNIT-I: Introduction

Information Source, Symbols, and Entropy, Mutual information, information Measures for Continuous Random Variable, Joint and Conditional Entropy, Relative Entropy, Applications Based on information Theoretic Approach.

UNIT-II: Source coding

Source Coding Theorem, Kraft inequality, Shannon-Fano Codes, Huffman Codes, Run Length Code, Arithmetic Codes, Lempel-Ziv-Welch Algorithm, Universal Source Codes, Prefix Codes, Variable Length Codes, Uniquely Decodable Codes, instantaneous Codes, Shannon's Theorem, Shannon Fano Encoding Algorithm, Shannon's Noiseless Coding Theorem, Shannon's Noisy Coding Theorem.

UNIT-III: Communication channel

Channel and its Capacity, Continuous and Gaussian Channels, Discrete Memory-Less Channels, Symmetric Channel, Binary Erasure Channel, Estimation of Channel Capacity, Noiseless Channel, Channel Efficiency, Shannon's Theorem on Channel Capacity, Mimo Channels, Channel Capacity with Feedback.

UNIT-IV: Video and speech coding

Video Coding Basics, Quantization, Symbol Encoding, Intraframe Coding, Predictive Coding, Transform Coding, Subband Coding, Vector Quantization, Interframe Coding, Motion Compensated Coding, Image Compression, Jpeg, LZ78 Compression, Dictionary Based Compression, Statistical Modelling, Speech Coding, Psycho-Acousting Modelling, Time Frequency Mapping Quantization, Variable Length Coding, Multichannel Correlation and Irrelevancy, Long Term Correlation, Pre-Echo Control, Bit Allocation.

UNIT-V: Error control coding

Overview of Field, Group, Galois Field, Types of Codes, Hamming Weight, Minimum Distance Based Codes, Error Detection and Error Correction Theorems, Maximum Likelihood Decoder, Map Decoder, Linear Block Codes and Their Properties, Equivalent Codes, Generator Matrix and Parity Check Matrix, Systematic Codes, Cyclic Codes, Convolution Codes and Viterbi Decoding Algorithm, Iterative Decoding, Turbo Codes and Low Density-Parity-Check Codes, Asymptotic Equipartition Property, Bch Codes, Generator Polynomials, Decoding of Bch Codes, Reed Solomon Codes, Trellis Codes, Space Time Coding.

TEXT BOOKS:

1. T.M. Cover and J.A. Thomas, Elements of Information Theory, John Wiley & Sons.
2. Todd K. Moon, Error Correction coding, John Wiley, 2005.

REFERENCE BOOKS:

1. Shu lin/ Daniel J.Costello Jr., Error Control Coding, Prentice Hall series in computer applications in electrical engineering series (2/e) 2005.
2. Ranjan Bose, Information Theory, coding and cryptography (2/e), McGraw Hill

COURSE OUTCOMES:

1. Understand and compute entropy, mutual information, and related measures.
2. Apply and analyse source coding algorithms for efficient data compression.
3. Evaluate channel capacity and efficiency in communication systems.
4. Implement and compare video/speech coding and multimedia compression techniques.
5. Design and analyse error control codes for error detection and correction

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II Semester	IOT AND ITS COMMUNICATION PROTOCOLS (D2523801)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. Introduce the core architecture and technologies of IoT, including devices, gateways, networking, data management, and services.
2. Familiarize students with IoT reference architectures, views, and the design constraints encountered in real-world implementations.
3. Understand data link and network layer protocols that support communication in IoT systems, including both traditional and IoT-specific protocols.
4. Explore transport and session layer protocols essential for reliable and efficient data transfer in IoT communication models.
5. Explain service layer and security protocols used in IoT systems, emphasizing interoperability and secure communication.

UNIT-I

Introduction: IoT architecture outline, standards - IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service (XaaS), M2M and IoT Analytics

UNIT-II

IoT Reference Architecture: Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints-Introduction, Technical Design constraints

UNIT-III

IoT Data Link Layer & Network Layer Protocols: PHY/MAC Layer (3GPP MTC, IEEE 802.11, IEEE 802.15), Wireless HART, Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH7 - Network Layer-IPv4, IPv6, 6LoWPAN, 6TiSCH, ND, DHCP, ICMP, RPL, CORPL, CARP

UNIT -IV

IoT Transport & Session Layer Protocols: Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, CoAP, XMPP, AMQP, MQTT

UNIT -V

IoT Service Layer Protocols & Security Protocols: Service Layer -oneM2M, ETSI M2M, OMA, BBF – Security in IoT Protocols – MAC802.15.4 , 6LoWPAN, RPL, Application Layer.

TEXT BOOKS:

1 Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications", ISBN: 978-1-118-47347-4, Willy Publications ,2016.

2 Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Aves and, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2015.

REFERENCE BOOKS

1. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642 19156-5 e-ISBN 978-3-642-19157-2, Springer, 2016.
2. N. Ida, Sensors, Actuators and Their Interfaces, Scitech Publishers, 2014.

COURSE OUTCOMES:

1. Understand the fundamental components and architecture of IoT systems.
2. Interpret and apply various IoT reference architectural views.
3. Analyse datalink and network layer protocols used in IoT communication
4. Evaluate transport and session layer protocols for their suitability in IoT applications
5. Assess IoT service layer and security protocols to ensure interoperability and secure communication

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II Semester	EMBEDDED SYSTEM DESIGN (D2523802)	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

1. To introduce the fundamentals, classification, and characteristics of embedded systems.
2. To explore the core components of embedded systems including processors, memory, and interfaces.
3. To understand embedded firmware components and design approaches.
4. To study ARM processor architecture, instruction sets, and programming model.
5. To provide practical exposure to Raspberry Pi programming, communication protocols, and sensor interfacing.

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT- II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

ARM: ARM design philosophy, data flow model and core architecture, registers, program status register, instruction pipeline, interrupts and vector table, operating modes and ARM processor families. Instruction Sets: Data processing instructions, addressing modes, branch, load, store instructions, PSR instructions, and conditional instructions.

UNIT -V

Raspberry Pi: Raspberry Pi board and its processor, Programming the Raspberry Pi using Python, Communication facilities on Raspberry Pi (I2C, SPI, UART), Interfacing of sensors and actuators.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.
2. A. N. Sloss, D. Symes, and C. Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Elsevier, 2008.
3. S. Monk, "Programming the Raspberry Pi" McGraw-Hill Education, 2013.

REFERENCE BOOKS:

1. Steave Furber, "ARM system-on-chip architecture", Addison Wesley, 2000.
2. Embedded Systems - Raj Kamal, TMH.
3. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Describe the structure, classification, and purpose of embedded systems and their quality attributes.
2. Analyse embedded system components such as processors, memory types, sensors, actuators, and interfaces.
3. Explain embedded firmware building blocks and apply suitable design approaches.
4. Demonstrate knowledge of ARM architecture and instruction sets relevant to embedded programming.
5. Develop simple embedded applications using Raspberry Pi and interface sensors and communication peripherals.

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II Semester	DESIGN FOR TESTABILITY (D25238A0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamental concepts, types, and philosophies of VLSI testing.
2. To familiarise fault models and apply logic/fault simulation techniques for test evaluation.
3. To study testability measures and design-for-test (DFT) techniques including scan design.
4. To explore Built-In Self-Test (BIST) strategies and their application in digital systems.
5. To learn the boundary scan architecture and standards used in board-level testing.

UNIT-I: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III: Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V: Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

2. VLSI Test Principles and Architectures: Design for Testability" – L.-T. Wang, C.-W. Wu, X. Wen

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

COURSE OUTCOMES:

1. Explain the role of testing in VLSI systems and differentiate between fault models and testing types.
2. Apply simulation algorithms for design verification and fault analysis in digital circuits.
3. Evaluate testability using measures like SCOAP and design scan-based test structures.
4. Design and implement BIST strategies for logic and memory testing.
5. Demonstrate understanding of boundary scan standards and describe systems using BSDL.

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II Semester	MEMS (D25238A1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamentals, materials, and applications of MEMS and smart systems.
2. To explore various types of micro-sensors, actuators, and smart material-based systems.
3. To study micro-fabrication techniques including deposition, lithography, and micromachining.
4. To understand the mechanical modelling of microstructures such as beams, bars, and multilayer elements.
5. To apply numerical analysis techniques like Finite Element Method (FEM) for modelling MEMS structures.

UNIT-I

Introduction to MEMS: Microsystems versus MEMS, Micro fabrication, Smart Materials, Structures and Systems, Integrated Microsystems, Applications of Smart Materials and Microsystems

UNIT-II

Micro Sensors, Actuators, Systems and Smart Materials: Silicon Capacitive Accelerometer, Piezo-resistive Pressure Sensor, Conductometric Gas Sensor, An Electrostatic Comb-Drive, A Magnetic Micro relay, Portable Blood Analyzer, Piezoelectric Inkjet Print Head, Micro-mirror Array for Video Projection Smart Materials and Systems

UNIT -III

Micro Fabrication Technique: Silicon as a Material for Micromachining, Thin-Film Deposition, Lithography, Etching, Silicon Micromachining Specialized Materials for Microsystems, Advanced Processes for Micro fabrication

UNIT-IV

Modeling Of Solids in Microsystems: The Simplest Deformable Element: A Bar, Transversely Deformable Element: A beam, Energy Methods for Elastic Bodies, Heterogeneous Layered Beams, Bimorph Effect, Residual Stresses and Stress Gradients, Poisson Effect and the Anticlastic Curvature of Beams, Torsion of Beams and Shear Stresses, Dealing with Large Displacements, In-Plane Stresses

UNIT-V

Finite Element Method: Need for Numerical Methods for Solution of Equations - Variational Principles, Finite Element Method, Finite Element Model for Structures with Piezoelectric Sensors and Actuators, Analysis of a Piezoelectric Bimorph Cantilever Beam

TEXT BOOKS:

1. Fundamentals of Microfabrication — *Marc J. Madou* (CRC Press, 1997/2002).
2. An Introduction to Microelectromechanical Systems Engineering — N. Maluf (Artech House, 1999).

REFERENCE BOOKS:

1. Micro and Smart Systems by G.K. Ananthasuresh, K.J. Vinoy, S.Gopalakrishnan, K.N.Bhat, V.K.Aatre: Wiley, India (2016).

2. Smart Material Systems and MEMS: Design and Development Methodologies: Vijay K., 2017 The MEMS Handbook: Edited by Mohamed Gad-el-Hak, University of NotreDame, CRC Press LLC, 2015

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Describe the basic concepts of MEMS, microfabrication, and smart materials.
2. Identify and explain the working principles of micro-sensors, actuators, and MEMS devices.
3. Demonstrate knowledge of various micro-fabrication processes used in MEMS manufacturing.
4. Analyse mechanical behaviour of MEMS structures using energy methods and elasticity concepts.
5. Apply FEM techniques for modelling and simulation of MEMS devices with piezoelectric elements.

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II Semester	SYSTEM ON CHIP DESIGN (D25238A2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamentals of SoC architecture, components, and design methodologies.
2. To understand hardware-software co-design concepts including partitioning, scheduling, and hardware acceleration.
3. To explore virtual prototyping, high-level synthesis, and system-level design methodologies.
4. To examine SoC interconnection structures and protocols like AMBA AXI and Network-on-Chip (NoC).
5. To analyse performance and power at the system level using simulation platforms and case studies.

UNIT-I: SoC Design Approach: Basics of Chips and SoC ICs, SoC Design: SoC CPU/IP Cores, Co-processor, Cache, DRAM Controller, SoC Synthesis, Static Timing Analysis (STA), Design for Testability, Verification, Physical Design.

UNIT-II:
Hardware-Software Co-Synthesis: Partitioning, Cycle Time, Die Area and Cost, Power, Area-Time-Power Trade-offs and Chip Reliability, Real-Time Scheduling, Hardware Acceleration.

UNIT-III: Virtual Prototyping and High-Level Synthesis (HLS): Mapping High-Level Language Applications to Hardware, Transaction-Level Modeling and Electronic System-Level Languages, Hardware Accelerators, Media Instructions, Coprocessors, System-Level Design Methodology, High-Level Synthesis (C-to-RTL), Hardware Synthesis and Architecture Techniques, Source-Level Optimizations.

UNIT-IV: SoC Interconnection Structures: Bus-Based Interconnection, Bus Protocols: AMBA AXI Bus, AXI4-Stream, IBM Core Connect, Avalon. Interconnection Structures, Network on Chip (NoC) Interconnection and NoC Systems, IP Interfacing.

UNIT-V: Performance/Power Analysis of SoCs: System-Level Modeling and Integration, Simulation Platform for Performance Analysis of SoC/MPSoC, Use Cases and Examples.

TEXT BOOKS:

1. Veena Chakravarthi, A Practical Approach to VLSI System on Chip (SoC) Design – A Comprehensive Guide, Springer, 2020
2. S. Pasricha and N. Dutt, On-Chip Communication Architectures: System on Chip Interconnect, Morgan Kaufmann–Elsevier Publishers, 2008

REFERENCE BOOKS:

1. Keating, M., The Simple Art of SoC Design, Springer, 2011.
2. "Embedded System Design: A Unified Hardware/Software Approach" Authors: Frank Vahid and Tony Givargis, Publisher: Wiley

COURSE OUTCOMES:

At the end of the course, students will be able to:

1. Understand and estimate key design metrics and requirements including area, latency, throughput, energy, and power.
2. Implement both hardware and software solutions, formulate hardware/software trade-offs, and perform hardware/software co-design.
3. Analyse issues in system-on-chip design associated with interconnection structures, performance, and power consumption.
4. Use System C programming and high-level synthesis (HLS) for design and modelling.
5. Design and optimize a modern System-on-a-Chip.

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II Semester	DETECTION AND ESTIMATION THEORY (D25238B0)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce fundamental concepts of random processes including Markov models, point processes, and Gaussian processes.
2. To develop understanding of detection theory using Bayesian and Neyman-Pearson approaches for signal classification under uncertainty.
3. To explore MMSE estimation techniques such as Wiener and Kalman filters for linear and nonlinear systems.
4. To provide knowledge of statistical inference including hypothesis testing, distribution estimation, and regression analysis.
5. To enable parameter estimation of random processes using model-free and model-based approaches with spectral analysis tools.

UNIT –I

Random Processes: Discrete Linear Models, Markov Sequences and Processes, Point Processes, and Gaussian Processes.

UNIT –II

Detection Theory: Basic Detection Problem, Maximum A posteriori Decision Rule, Minimum Probability of Error Classifier, Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal a priori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT –III

Linear Minimum Mean-Square Error Filtering: Linear Minimum Mean Squared Error Estimators; Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT –IV

Statistics: Measurements, Nonparametric Estimators of Probability Distribution and Density Functions, Point Estimators of Parameters, Measures of the Quality of Estimators, Introduction to Interval Estimates, Distribution of Estimators, Tests of Hypotheses, Simple Linear Regression, Multiple Linear Regression.

UNIT –V

Estimating the Parameters of Random Processes from Data: Tests for Stationarity and Ergodicity, Model-free Estimation, Model-based Estimation of Autocorrelation Functions, Power Special Density Functions.

TEXT BOOKS:

1. Steven M. Kay, "Fundamentals of Statistical signal processing, volume 1: Estimation theory". Prentice Hall 2011.
2. Steven M. Kay, "Fundamentals of Statistical signal processing, volume 2: Detection theory". Prentice Hall 2011.

REFERENCE BOOKS:

1. Harry L. Van Trees, "Detection, Estimation, and Modulation Theory, Part I," John Wiley & Sons, Inc. 2011
2. A. Papoulis and S. Unnikrishna Pillai, "Probability, Random Variables and stochastic processes, 4e". The McGraw-Hill 2010

COURSE OUTCOMES:

1. Demonstrate understanding of random processes, including discrete linear models, Markov processes, point processes, and Gaussian processes relevant to signal processing.
2. Apply detection theory to solve problems using MAP, Bayes, and Neyman-Pearson decision rules for both binary and multiple hypothesis testing.
3. Develop and analyze linear and nonlinear minimum mean square error (MMSE) estimators, and design digital Wiener and Kalman filters for signal estimation.
4. Estimate and interpret statistical parameters and distributions using point estimation, nonparametric methods, interval estimates, hypothesis testing, and linear regression models.
5. Evaluate stationarity and ergodicity of random processes and perform both model-free and model-based estimation of autocorrelation and power spectral density functions from data.

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II Semester	EMI/ EMC (D25238B1)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce enough knowledge regarding the Electromagnetic interference/ Electromagnetic compatibility, Its practical experiences and concerns, and various sources both the natural and nuclear sources of EMI.
2. To know the practical experiences due to EMI such as mains power supply, switches and relays etc and Analyse EM Propagation and Crosstalk
3. To know various methods of the measurements radiated and conducted interference in open area test sites and in chambers.
4. To Learn about the various methods of minimizing the EMI.
5. To know the National/International EMC Standards.

UNIT -I: Introduction, Natural and Nuclear Sources of EMI / EMC:
Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations, An overview of EMI / EMC, Natural and Nuclear sources of EMI.

UNIT -II: EMI from Apparatus, Circuits and Open Area Test Sites:
Electromagnetic emissions, Noise from relays and switches, non-linearities in circuits, passive intermodulation, Cross talk in transmission lines, Transients in power supply lines, Electromagnetic interference (EMI), Open area test sites and measurements.

UNIT -III: Radiated and Conducted Interference Measurements and ESD:
Anechoic chamber, TEM cell, GH TEM Cell, Characterization of conduction currents / voltages, Conducted EM noise on power lines, Conducted EMI from equipment, Immunity to conducted EMI detectors and measurements, ESD, Electrical fast transients / bursts, Electrical surges.

UNIT -IV: Grounding, Shielding, Bonding and EMI filters:
Principles and types of grounding, Shielding and bonding, Characterization of filters, Power lines filter design.

UNIT -V: Cables, Connectors, Components and EMC Standards:
EMI suppression cables, EMC connectors, EMC Gas kets, Isolation Transformers, optoisolators, National / International EMC standards.

TEXT BOOKS:

1. Engineering Electromagnetic Compatibility - Dr. V.P. Kodali, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
2. Electromagnetic Interference and Compatibility IMPACT series, IIT – Delhi, Modules 1-9

REFERENCE BOOKS:

1. Introduction to Electromagnetic Compatibility - Ny, John Wiley, 1992, by C.R. Pal.

COURSE OUTCOMES:

At the end of this course the student can able to:

1. Understand the electromagnetic environment the definitions of EMI and EMC, history of EMI some examples of practical experiences due to EMI such as mains power supply, switches and relays etc.
2. Understand the celestial electromagnetic noise the occurrence of lightning discharge and their effects, the charge accumulation and discharge in an electrostatic discharge, model ESD wave form, the various cases of nuclear explosion and the transients.
3. Understand the methods to measure RE and RS in the open are test sites.
4. Understand the measurement facilities and procedures using anechoic chamber, TEM cell, reverberating chamber GTEM cell.
5. Apply grounding, shielding, bonding techniques, and design EMI filters for interference mitigation.

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II Semester	ARM CONTROLLERS AND EMBEDDED C (D25238B2)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce ARM processor architecture, instruction sets, and efficient programming techniques.
2. To explore exception handling, memory hierarchy, and management units in ARM systems.
3. To develop embedded system applications using ARM Cortex-M microcontrollers.
4. To implement peripheral interfacing techniques including UART, ADC/DAC, and GPIO.
5. To understand communication protocols like I²C and SPI through practical case studies.

UNIT- I: ARM Processor Fundamentals: ARM Design Philosophy, Registers, CPSR, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions.

Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Load Store Instructions, Software Interrupt Instruction, PSR Instructions.

Introduction to the Thumb Instruction Set: Thumb Register Usage, Branch Instructions, Data Processing Instructions, Load-Store Instructions, Stack instructions, Software Interrupt Instruction.

Efficient C Programming: Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Structure Arrangement.

Writing and Optimizing ARM Assembly Code: Writing Assembly Code, Profiling and Cycle Counting, Instruction Scheduling, Register Allocation, Conditional Execution, Looping Constructs.

UNIT -II: Exception and Interrupt Handling: Exception Handling, Interrupts, Interrupt Handling Schemes

Caches: The Memory Hierarchy and Cache Memory, Cache Architecture, Cache Policy, Flushing and Cleaning Cache Memory.

Memory Protection Units: Protected Regions, Initializing the MPU, Caches and Write Buffer.

Memory Management Units: Moving from an MPU to an MMU, How Virtual Memory Works, Details of the ARM MMU, Page Tables, Translation Lookaside Buffer, Domains And Memory Access Permission, The Fast Context Switch Extension

UNIT- III: Introduction: Definition of Embedded Systems, Real life examples of embedded systems, Basics of Developing for Embedded Systems.

ARM Instruction set Architecture: ARM Cortex-M Organization, Arithmetic, Logical and Shift instructions, Data Movement Instructions, Branch instructions, Program Status register,

Bitwise logic operations, Sign and Zero extension, Data Comparison, Memory addressing, Branch and conditional execution, Control structures, Subroutines, 64-bit data processing.

GPIO: GPIO Input Modes, GPIO Output Modes, Memory-mapped I/O, Push button, Programming exercises on GPIO and Push-button
General-purpose Timers: Clock Configuration, Timer Organization, and Counting Modes, Timer Update Events, PWM Registers, Configuration and initialization of PWM block, Programming exercises on the selection of clock source, Timer's concept, and PWM

UNIT-IV: UART: UART Block, UART Registers, UART baud rate calculation, Configuration and initialization of UART.
ADC/DAC: ADC & DAC registers, pin configuration, ADC modes, Configuring ADC and DAC module, Programming exercises on ADC and DAC
Interfacing: Keypad, LCD, and Seven segment display interfacing with ARM Cortex-M3 Microcontroller

UNIT-V:
Inter-Integrated Circuit (I^2C): I^2C operating modes, Configuration of I^2C, Interface a sensor using I^2C protocol. **Serial Peripheral Interface (SPI):** SPI Modes, Master operation, Slave operation, Configuration of SPI. **Case Study:** Smart Home-Smart Door Locks and Interface a temperature sensor with an I^2C Module to measure the room temperature.

TEXT BOOKS:

1. A.Sloss, D.Symes, C.Wright, "ARM system Developers Guide: Designing and Optimizing System Software", Morgan Kaufmann publishers, 2012.
2. Dr.Yifeng Zhu "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly and C" Third edition, 2018

REFERENCE BOOKS:

1. Steve Furber, "ARM System on Chip Architecture", 2nd ed., Addison Wesley Professional,2000.
2. Valvano, J,"Embedded microcomputer systems: real time interfacing", 3rd Edition, Cengage Learning, 2011.
3. Frank Vahid, TonyGivargis, "Embedded System Design", J Wiley India,2005.
4. Ariel Lutenberg, Pablo Gomez, Eric Pernia "A Beginner's Guide to Designing Embedded System Applications on Arm Cortex-M Microcontrollers"
5. Qing Li, Caroline Yao "Real-time concepts for Embedded Systems" CMP books.

COURSE OUTCOMES:

1. Demonstrate proficiency in ARM instruction sets and assembly code optimization.
2. Configure and manage exceptions, interrupts, and memory systems in ARM-based designs
3. Develop embedded applications using GPIO, timers, and control structures.
4. Interface and program peripherals such as UART, ADC/DAC, and display modules.
5. Apply I²C and SPI protocols in real-world scenarios like smart home systems

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II Semester	INTERNET OF THINGS LAB (D2523803)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To introduce students to the fundamentals of IoT architecture and physical layer components.
2. To familiarize students with sensors, actuators, transducers, microcontrollers, and microprocessors used in IoT.
3. To provide hands-on experience with Arduino, Scratch programming, S4A tool, and Arduino IDE.
4. To develop practical skills using Tinker cad simulations and real-time Arduino-based interfaces.
5. To enable interfacing of digital and analog sensors and actuators with Arduino for real-time applications.

List of Experiments:

1. Introduction to IoT, IoT Architecture, introduction to Physical layer
2. Introduction to sensors, actuators, and transducers. Introduction to microcontrollers and microprocessors
3. Introduction to Arduino. Introduction to Scratch programming, S4A tool, and Arduino IDE.
4. Introduction to Tinker cad and some practical examples
5. Working with analog, digital inputs & outputs
6. Interfacing Arduino with Embedded sensors and Actuators
7. Interfacing Arduino with additional sensors
8. Working on Displays and interfacing with Arduino
9. Arduino & LCD Based Projects
10. Arduino interfacing with Keypad and its operation
11. Creating the app (app designing using MIT) and controlling your hardware with your app.
12. Introduction to Node MCU and basic tasks
13. Introduction to Cloud, some IoT Cloud Platforms publishing sensor data to a cloud using Thing speak
14. Controlling your sensor data using Thing speak and MIT APP Inventor
15. Email notifications, app alerts using Blynk cloud
16. Home Automation Using Blynk app

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COURSE OUTCOMES:

At the end of the Course the student shall be able to

1. Analyze the concepts of IoT along with its applications.
2. Design a prototype using Arduino Uno.
3. Analyze different types of sensors, actuators and communication Protocols.
4. Execute a prototype of Home Automation using Blynk app.
5. Design an IoT application to interact with cloud.

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II Semester	EMBEDDED SYSTEM DESIGN LAB (D2523804)	L	T	P	C
		0	1	2	2

COURSE OBJECTIVES:

1. To introduce students to GPIO configuration and control in embedded systems.
2. To develop skills in serial communication between microcontrollers and PCs using UART.
3. To understand timer and counter functionalities for time delays and interrupts.
4. To provide experience with LCD interfacing and real-time message display.
5. To implement analog-to-digital conversion and PWM signal generation for control applications.

Experiments using ARM Cortex-M Microcontroller: (NUCLEO board -F429ZI):

1. Program to configure and control General Purpose Input / Output (GPIO) port pins.
2. Program to demonstrate Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
3. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment.
4. Program to demonstrate a simple interrupt handler and setting up a timer.
5. Program to Displaying a message in a 2-line x 16 Characters LCD display and verify the result in debug terminal.
6. Program to demonstrate ADC interfacing.
7. Generation of PWM Signal with the objective of introducing the practical application of timers and fundamental principles of control theory.
8. To integrate a micro-SD card with the computing system for the purpose of storing event logs conveniently on the SD card.
9. To establish a connection between the two computing systems using Bluetooth Low Energy (BLE), with the objective of monitoring pertinent information from one system and facilitating gate control through the other system.
10. To enhance the smart home system by enabling it to host a web page through Wi-Fi connectivity, thereby allowing users to access information using a smartphone or PC.

COURSE OUTCOMES:

After successful completion of this lab course, students will be able to:

1. Configure and control GPIO ports and interface with external devices.
2. Implement UART-based serial communication and use debug terminals for testing.
3. Apply timers and counters for generating delays and handling interrupts in real-time systems.
4. Interface LCDs, ADC modules, and generate PWM signals for embedded applications.
5. Store and retrieve event data using SD card integration.

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II Semester	SEMINAR – II (D2523804)	L	T	P	C
		0	0	2	1

For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

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III Semester	RESEARCH METHODOLOGY AND IPR (D2530000)	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

1. To introduce the fundamentals of research methodology, including research design and problem formulation.
2. To develop skills for effective literature review, data collection, analysis, and technical writing.
3. To enhance understanding of ethical issues and plagiarism in research.
4. To provide an overview of intellectual property rights, including patents, copyrights, trademarks, and trade secrets.
5. To create awareness about the process of filing IPR and its role in innovation, entrepreneurship, and academic research.

UNIT-I: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II: Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-III: Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV: Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent information and databases, Geographical Indications.

UNIT-V:

New Developments in IPR: Administration of Patent System. New developments in IPR, IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCES:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
3. Mayall, "Industrial Design", McGraw Hill,1992.
4. Niebel, "Product Design", McGraw Hill,1974.
5. Asimov, "Introduction to Design", Prentice Hall,1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New TechnologicalAge",2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008

COURSE OUTCOMES:

At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information and Follow research ethics
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

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III Semester	SUMMER INTERNSHIP /INDUSTRIAL TRAINING (D2533801)	L	T	P	C
		0	0	0	3

Students shall undergo mandatory summer internship / industrial training (3 credits) for a minimum of eight weeks duration at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before the committee. The Committee comprises of a HoD / Professor of the department and two faculty. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

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III Semester	COMPREHENSIVE VIVA# (D2533802)	L	T	P	C
		0	0	0	2

The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. The examination committee will be constituted by the HoD and Professor of the department and two faculty. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

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III Semester	DISSERTATION PART– A^{S} (D2533804)	L	T	P	C
		0	0	20	10

IV Semester	DISSERTATION PART– B% (D2543800)	L	T	P	C
		0	0	32	16

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DR25

M.Tech

Other Department Subject

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

I Year-I Semester M. Tech (Machine Design)	VISION SYSTEMS AND IMAGE PROCESSING (Programme Elective –II)	L	T	P	C
		3	0	0	3

Course Outcomes:

- Understand basics of machine vision systems and applications.
- Explain image representation and transformation techniques.
- Apply spatial and frequency domain image processing methods.
- Analyse image enhancement and segmentation techniques.
- Evaluate image compression and image analysis methods.

UNIT-I:
Machine vision: Vision sensors - Comparison with other types of sensors- Image acquisition and recognition - Recognition of 3D objects – Lighting techniques - Machine vision applications.

UNIT-II:
Image representation: Application of image processing - Image sampling, Digitization and quantization - Image transforms.

UNIT-III:
Spatial domain techniques: Convolution, Correlation. Frequency domain operations - Fast Fourier transforms, FFT, DFT, Investigation of spectra. Hough transforms.

UNIT-IV:
Image enhancement: Filtering, Restoration, Histogram equalisation, Segmentation, Region growing.

UNIT-V:
Image compression: Edge detection - Thresholding - Spatial smoothing - Boundary and Region representation - Shape features - Scene matching and detection - Image classification.

TEXT BOOKS:

1. Digital Image Processing by Gonzalez, R.C. and Woods, R.E., Addison Wesley Publications.
2 Robot Vision by Prof. Alan Pugh (Editor), IFS Ltd., U.K.
3. Digital Image Processing by A. Rosenfled and A. Kak, Academic Press.

REFERENCES:

1. The Psychology of Computer Vision by P. Winstan, McGraw-Hill.
2. Algorithms for Graphics and Image Processing by T. Pavidis, Springer Verlag.

e-RESOURCES:

- https://nptel.ac.in/courses/117105079.
- https://ocw.mit.edu/courses/6-801-machine-vision-fall-2004.

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Annexure-C

DR24
B.Tech
Model Papers

Course Code: BT24EC3101

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B. Tech. I Semester MODEL QUESTION PAPER

ANALOG AND DIGITAL IC APPLICATIONS

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	Draw the Pin diagram of Op-Amp.	1	2	2
	b).	Define CMRR.	1	3	2
	c).	Draw the circuit diagram of first order HPF using op-amp	2	2	2
	d).	Draw the circuit diagram of current to voltage converter using op-amp	2	1	2
	e).	Draw the Pin diagram of 555 timer.	3	1	2
	f).	Mention any 4 applications of 555 Timer as Monostable multivibrator.	4	2	2
	g).	What are the different types of DACs?	5	2	2
	h).	List important specifications of ADC.	5	1	2
	i).	Draw the circuit diagram of Decoder using 74x138.	6	2	2
	j).	Draw the Pin diagram of IC 7476.	6	1	2
				5 x 10 = 50 Marks	
		UNIT-1			
2.	a).	Draw a block diagram of typical OP-AMP and explain the function of each block.	1	3	5
	b).	Explain the operation of Square wave generator circuit with neat circuit diagram and derive expression for time period.	1	4	5
		OR			
3.	a).	Explain the operation of a Regenerative comparator with circuit diagram and Waveforms.	1	2	4
	b).	Explain the operation of any 2 of the following op amp applications. (i) Differentiator (ii) Summing amplifier (iii) Logarithmic amplifier	1	4	6
		UNIT-2			
4.	a).	Derive the transfer function of a second order LPF. Comment on its frequency response.	2	3	5
	b).	Draw the basic circuit of an op amp based RC phase shift oscillator and explain its operation. Also, derive the expression for frequency of	2	4	5

		oscillation.			
		OR			
5.	**a).**	Design voltage to current converter using op-amp and then explain its operation.	**2**	**3**	**5**
	b).	Draw the op amp based bandpass filter circuit and briefly explain about its operating principle along with its frequency response curve.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Draw the circuit of Schmitt trigger using IC555 timer and explain its operation?	**3**	**3**	**5**
	b).	Draw and explain the working of 555-timer circuit in astable mode to get output waveform with 50% duty cycle.	**3**	**4**	**5**
		OR			
7.	**a).**	List important specifications of 566 VCO IC.	**4**	**3**	**5**
	b).	With the help of schematic diagram of 555 timer, explain how it can be used as mono stablemultivibrator	**4**	**4**	**5**
		UNIT-4			
8.	**a).**	With a neat diagram explain the working principle of R-2R ladder type DAC.	**5**	**3**	**5**
	b).	With a neat block diagram, explain successive approximation type A/D converters in detail.	**5**	**3**	**5**
		OR			
9.	**a).**	Which is the fastest ADC? Explain the operation and discuss its merits and demerits.	**5**	**3**	**5**
	b).	Draw and explain the circuit diagram of parallel comparator type ADC.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Design an asynchronous Decade counter using IC 7476 and explain the operation.	**6**	**4**	**5**
	b).	Explain the following Sequential logic circuits with suitable ICs. (a) Multiplexer. (b) Priority Encoder.	**6**	**3**	**5**
		OR			
11.	**a).**	Explain the following Combinational logic circuits with suitable ICs. (a) D flip-flop. (b) JK Flip-flop.	**6**	**3**	**5**
	b).	Design a Universal shift Register using IC74X194 and explain the operation.	**6**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

Head
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Course Code: BT24EC3103

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

ANTENNAS & WAVE PROPAGATION

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	Define Half Power Beam Width.	1	2	2
	b).	What is meant by Polarization? And its types.	1	1	2
	c).	List out the salient features of antenna array?	2	2	2
	d).	What is meant by array factor?	2	1	2
	e).	What are the advantages of microstrip antenna?	3	1	2
	f).	What is Spill over and back lobe radiation	4	1	2
	g).	What are the possible errors in antenna measurements?	5	2	2
	h).	What are the methods to measure Phase of an antenna?	5	1	2
	i).	Define wave tilt	6	1	2
	j).	Find the range of LOS system when they receive and transmit antenna heights are 10m and 100m respectively.	6	3	2
		5 x 10 = 50 Marks			
		UNIT-1			
2.	a).	Derive expressions for the EM fields radiated by a $\lambda/2$ Dipole.	1	3	5
	b).	Discuss the Radiation characteristics of dipole antennas	1	2	5
		OR			
3.	a).	Compute the radiation resistance of a Quarter wave Monopole.	1	3	5
	b).	Explain about different types of current distribution on linear Antennas.	1	2	5
		UNIT-2			
4	a)	Obtain expressions for BWFN and HPBW in Broad-side array.	2	3	5
	b)	Show that in a Uniform linear array, the first side lobe is down the principal maximum by 13.5 db	2	3	5
		OR			
5.	a)	Derive the Electric field radiated by a two element uniform linear array.	2	3	5
	b)	Explain the technique of pattern multiplication with examples	2	2	5

		UNIT-3			
6.	**a).**	With a neat diagram, explain the operating principles of Log periodic Antenna. List out the disadvantages of a Log periodic Antenna	**3**	**2**	**5**
	b).	Obtain Design parameters of Yagi Uda antenna to operate at 30 MHz.	**3**	**4**	**5**
		OR			
7.	**a).**	Explain in detail the operating principles of Helical antenna.	**4**	**2**	**5**
	b).	Derive an expression for the expression of the impedance of the Slot Antenna.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	Explain in detail about the slotted line method of antenna input Impedance measurement.	**5**	**2**	**5**
	b).	Explain the method of measuring the radiation pattern of an antenna.	**5**	**2**	**5**
		OR			
9.	**a).**	Explain the measurement of antenna gain using two antenna method.	**5**	**2**	**5**
	b).	Explain the method of measurement of phase of an antenna.	**5**	**2**	**5**
		UNIT-5			
10.	**a).**	Derive an expression for the refractive index of the Ionosphere.	**6**	**2**	**5**
	b)	Explain ground wave propagation in detail.	**6**	**2**	**5**
		OR			
11.	**a).**	Derive an expression for the field strength of a Space wave.	**6**	**3**	**5**
	b).	Explain the terms Critical frequency, MUF and Skip distance.	**6**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: BT24EC3102

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

DIGITAL COMMUNICATIONS

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	State Nyquist Sampling theorem.	1	1	2
	b).	What is companding?	1	1	2
	c).	What is bit rate?	2	1	2
	d).	Draw the phasor diagram for the QPSK system.	2	1	2
	e).	Define Noise bandwidth.	3	1	2
	f).	Show that the coefficients of spectral components a_k and b_k are uncorrelated to each other.	4	2	2
	g).	What is a matched filter?	5	1	2
	h).	What is a correlator?	5	1	2
	i).	List any two advantages of spread spectrum modulation.	6	1	2
	j).	List any two applications of spread spectrum modulation.	6	1	2
					5 x 10 = 50 Marks
		UNIT-I			
2.	a).	Explain how the linear delta modulation can be used for baseband signal transmission. What are the limitations and how can they be eliminated?	1	2	5
	b).	Explain the operation of Differential Pulse Code Modulation (DPCM) with neat block diagrams.	1	2	5
		OR			
3.	a).	Explain the operation of a PCM system with the help of a neat block diagram and an example.	1	2	5
	b).	With the help of an example, explain the operation of a synchronous TDM-PCM system(T1-Digital System).	1	2	5
		UNIT-II			
4.	a).	Explain the operation of Binary Phase Shift Keying(BPSK) system with the help of neat block diagrams.	2	2	5
	b).	Explain the operation of Minimum Shift Keying (MSK) with neat block diagrams. Sketch the MSK waveforms for the given bit stream b(t)=	2	2	5

		0110100 for m = 5.			
		OR			
5.	**a).**	Explain the operation of Quadrature Phase Shift Keying(QPSK) system with the help of neat block diagrams.	**2**	**2**	**5**
	b).	In a DEPSK Receiver, the received bit sequence b(t) is 01101100 then i) Find reconstructed bit sequence d(t) ii)Due to the presence of noise b(t) is recovered as 01111100 then, detect d(t) and also identify the bits which are wrongly detected. Use EX-OR logic.	**2**	**3**	**5**
		UNIT-III			
6.	**a).**	Explain about linear filtering and calculate noise power output of RC low pass filter and an integrator.	**3**	**2**	**5**
	b).	Explain about frequency domain representation of noise.	**3**	**2**	**5**
		OR			
7.	**a).**	Explain some sources of noise and narrow band representation of noise.	**4**	**2**	**5**
	b).	What is the effect of filtering on power spectral density of noise and obtain the relation between H(f), input noise PSD $G_{ni(f)}$ & output noise PSD $G_{no(f)}$	**4**	**2**	**5**
		UNIT-IV			
8.	**a).**	Explain the function of a baseband signal receiver and derive its probability of error?	**5**	**2**	**5**
	b).	By deriving expression for P_e for BPSK and BFSK systems, compare the performance of these two data transmission systems	**5**	**3**	**5**
		OR			
9.	**a).**	Derive an expression of Probability of error P_e for an optimum filter.	**5**	**3**	**5**
	b).	Derive the expression of Probability of error P_e for a matched filter.	**5**	**3**	**5**
		UNIT-V			
10.	**a).**	Derive an expression for output SNR when the binary signal is transmitted using BPSK in a PCM system.	**6**	**3**	**6**
	b).	Compare the noise performance of PCM and DM systems.	**6**	**3**	**4**
		OR			
11.	**a).**	How a CDMA system uses DS Spread Spectrum to provide multiple access communication.	**6**	**2**	**5**
	b).	Explain the operation of Frequency Hopping Spread Spectrum with the help of a neat block diagram.	**6**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: BT24EC31P1C

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

ELECTRONIC MEASUREMENTS AND INSTRUMENTATION

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	What is meant by accuracy and precision in measurement?	1	2	2
	b).	Define and explain types of static errors.	1	2	2
	c).	What is a transducer? Give two examples.	2	2	2
	d).	Define active and passive transducers with examples.	2	2	2
	e).	What is an oscilloscope? Mention its basic purpose.	3	2	2
	f).	Define trigger pulse and sweep in CRO.	4	2	2
	g).	What is the purpose of using a Wheatstone bridge?	5	2	2
	h).	Write the applications of capacitance bridges.	5	2	2
	i).	What is a signal generator? Mention its use.	6	2	2
	j).	Define harmonic distortion analyzer.	6	2	2
		5 x 10 = 50 Marks			
		UNIT-1			
2.	a).	Define resolution and sensitivity in electronic instruments.	1	3	5
	b).	What is the significance of fidelity and lag in dynamic characteristics?	1	3	5
		OR			
3.	a).	List the types of DC and AC voltmeters and mention one application each.	1	3	5
	b).	Describe the working of a True RMS voltmeter.	1	4	5
		UNIT-2			
4.	a).	What are active and passive transducers? Give one example each.	2	2	5
	b).	State the principle of a piezoelectric transducer.	2	2	5
		OR			
5.	a).	What is a strain gauge? List two types.	2	2	5
	b).	How does a resistance thermometer measure temperature?	2	3	5
		UNIT-3			

6.	**a).**	Define sweep and trigger pulse in CRO.	**3**	**2**	**5**
	b).	What is a dual trace oscilloscope?	**3**	**2**	**5**
		OR			
7.	**a).**	List the features of a digital storage oscilloscope.	**4**	**3**	**5**
	b).	How is frequency measured using Lissajous patterns?	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	What is the purpose of a Wheatstone bridge?	**5**	**2**	**5**
	b).	List the precautions to be taken while using electrical bridges.	**5**	**2**	**5**
		OR			
9.	**a).**	Define the principle of a Schering bridge.	**5**	**2**	**5**
	b).	Mention one application each for inductance and capacitance bridges.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	List different types of signal generators and their outputs.	**6**	**3**	**5**
	b).	What is an arbitrary waveform generator?	**6**	**3**	**5**
		OR			
11.	**a).**	Differentiate between sine wave and square wave signal generators.	**6**	**3**	**5**
	b).	Define sweep generator and mention its use.	**6**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: BT24EC31P1A

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

DIGITAL SYSTEM DESIGN THROUGH HDL

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	What is the role of a module in Verilog HDL?	1	2	2
	b).	Define gate primitives in Verilog with one example.	1	2	2
	c).	What is a procedural assignment in Verilog behavioral modeling?	2	2	2
	d).	Differentiate between sequential and parallel blocks.	2	2	2
	e).	What is a continuous assignment in dataflow modeling?	3	2	2
	f).	List any two operators used in Verilog dataflow model.	4	2	2
	g).	What is the difference between Moore and Mealy machines?	5	2	2
	h).	Define a user-defined primitive (UDP) with a basic example.	5	2	2
	i).	What is a test bench in Verilog?	6	2	2
	j).	Define design verification.	6	2	2

5 x 10 = 50 Marks

		UNIT-1			
2.	a).	List different data types used in Verilog.	1	2	5
	b).	What are system tasks in Verilog? Give examples.	1	2	5
		OR			
3.	a).	Explain the purpose of tri-state gates in digital design.	1	2	5
	b).	What is the use of delay specification in gate-level modeling?	1	2	5
		UNIT-2			
4.	a).	What is the role of loops in behavioral modeling?	2	2	5
	b).	Explain conditional statements used in Verilog.	2	2	5
		OR			
5.	a).	How is a flip-flop designed using behavioral modeling?	2	3	5
	b).	Write a simple Verilog code for a 4-to-1 multiplexer using behavioral model.	2	3	5

		UNIT-3			
6.	**a).**	How are delays specified in continuous assignments?	**3**	**2**	**5**
	b).	Write a simple Verilog code for a decoder using dataflow modeling.	**3**	**3**	**5**
		OR			
7.	**a).**	What are the basic transistor switches used in switch-level modeling?	**4**	**2**	**5**
	b).	Differentiate between dataflow and behavioral modeling.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	What are the basic components of a state machine?	**5**	**2**	**5**
	b).	Write the advantages of using one-hot encoding in FSM design.	**5**	**2**	**5**
		OR			
9.	**a).**	What is the purpose of synthesis in digital design?	**5**	**3**	**5**
	b).	Explain the synthesis of sequential logic using flip-flops.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain the purpose of assertion verification.	**6**	**2**	**5**
	b).	How are combinational circuits tested using a test bench?	**6**	**2**	**5**
		OR			
11.	**a).**	Mention two techniques for testing sequential circuits.	**6**	**3**	**5**
	b).	Write a simple Verilog test bench to verify a 2-input AND gate.	**6**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: BT24EC31P1B

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

OPTICAL COMMUNICATIONS

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	**a).**	What is Numerical Aperture (NA) of an optical fiber and what is its significance?	**1**	**2**	**2**
	b).	Define V-number of an optical fiber and state its role in mode propagation.	**1**	**2**	**2**
	c).	What is attenuation in optical fibers? Mention any two causes.	**2**	**2**	**2**
	d).	Define material dispersion and state its effect on pulse broadening.	**2**	**2**	**2**
	e).	What is connector return loss in optical fiber connectors?	**3**	**2**	**2**
	f).	List any two fiber splicing techniques used in optical communication systems.	**4**	**2**	**2**
	g).	Define quantum efficiency of an optical source.	**5**	**2**	**2**
	h).	State two differences between PIN and APD photodiodes.	**5**	**2**	**2**
	i).	What is meant by link power budget in an optical communication system?	**6**	**2**	**2**
	j).	Define eye pattern and mention its importance in digital optical receivers.	**6**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Draw the structure of an optical fiber and explain each part. Why the cladding refractive index is less than core refractive index? Explain.	**1**	**2**	**5**
	b).	Calculate the cut-off wavelength for a SIF to exhibit single-mode-operation when the core refractive index and radius are 1.48 and 5μm respectively, with the relative index difference being 0.25%.	**1**	**2**	**5**
		OR			
3.	**a).**	Draw the block diagram of an optical fiber communication system and explain each part.	**1**	**2**	**5**
	b).	Define refractive index and explain the concept of Effective refractive index.	**1**	**2**	**5**
		UNIT-2			

4.	**a).**	Explain the designing and applications of Chalgenide glass fibers.	**2**	**2**	**5**
	b).	Explain the effect of dispersion on digital pulse transmitted in fiber with suitable diagrams.	**2**	**2**	**5**
		OR			
5.	**a).**	Discuss in detail about losses due to fiber bend.	**2**	**3**	**5**
	b).	Write a short note on Pulse broadening in Graded index fiber.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Explain about V-groove splicing technique with suitable diagrams.	**3**	**2**	**5**
	b).	Discuss about alignment Losses.	**3**	**3**	**5**
		OR			
7.	**a).**	Explain the designing and working of Expanded beam connectors.	**4**	**2**	**5**
	b).	Discuss about core-diameter mismatch and numerical aperture mismatch.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	In a 100ns pulse, 6x106 photons at a wavelength of 1330nm fall on an InGaAs photo detector. On the average 5X106 electron-hole pairs are generated. Find the Quantum efficiency.	**5**	**2**	**5**
	b).	Explain the working principle of a surface emitting LED.	**5**	**2**	**5**
		OR			
9.	**a).**	Discuss about threshold conditions in Laser diode.	**5**	**3**	**5**
	b).	List out the performances of different photo detectors.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Define Lambertian Pattern? Draw the radiation patterns radiated by different optical sources.	**6**	**2**	**5**
	b).	Explain Attenuation measurement using cutback technique with suitable diagrams.	**6**	**2**	**5**
		OR			
11.	**a).**	Explain about time-domain intermodal dispersion measurement	**6**	**3**	**5**
	b).	Classify and explain Line coding techniques used in Optical links.	**6**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: BT24EC31P1D

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

COMPUTER ORGANIZATION AND ARCHITECTURE

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	Explain about Bus structure.	1	2	2
	b).	What are the uses of system software?	1	2	2
	c).	Define instruction. Give its format.	2	2	2
	d).	What are four types of operations performed by computer instructions?	2	2	2
	e).	Write about additional considerations in additional addressing modes.	3	2	2
	f).	Write about general register organization.	4	2	2
	g).	Write the responsibilities of PCI bus in computer system.	5	2	2
	h).	What is the role of disk controller in secondary storage?	5	2	2
	i).	Discuss briefly about read only memory.	6	2	2
	j).	What is auxiliary memory?	6	2	2
		5 x 10 = 50 Marks			
		UNIT-1			
2.	a).	What is register transfer notation? Write and explain these notations to three address, two-address, single address and zero-address instruction types.	1	2	5
	b).	Draw and explain the basic block diagram of a digital computer. Also list the different types of computers.	1	2	5
		OR			
3.	a).	Name and explain three-address, two-address, one-address, and zero-address instructions with an example.	1	2	5
	b).	Explain the various Data types that are represented in computers with example.	1	2	5
		UNIT-2			
4.		What is purpose of Branch Instructions? List out Branch Instructions and write any example program using these Instructions	2	2	5
		OR			
5.	a).	Classify the instructions of typical computers. Explain about shift	2	3	5

		Instructions.			
	b).	Discuss hardware implementation for signed magnitude for addition and subtraction.	2	3	5
		UNIT-3			
6.	a).	What is a stack frame? Explain a commonly used layout for information in a subroutine stack frame	3	2	5
	b).	Perform the arithmetic operations (+42) + (-13) and (-42)- (-13) in binary using signed 2's complement representation for negative numbers.	3	3	5
		OR			
7.	a).	Demonstrate the design of a 4-bit Arithmetic unit with two selection variables, which performs the basic arithmetic functions.	4	2	5
	b).	Write a note on enabling and disabling interrupts.	4	3	5
		UNIT-4			
8.	a).	Explain about Direct Memory Access in detail.	5	2	5
	b).	With a neat sketch Explain Input-output processor.	5	2	5
		OR			
9.	a).	Distinguish between Synchronous Bus and Asynchronous Bus.	5	3	5
	b).	Explain about Peripheral component Interconnect (PCI)bus.	5	3	5
		UNIT-5			
10.	a).	Elaborate briefly about Associate-mapped and set-associate mapped cache.	6	2	5
	b).	Discuss different memory allocation techniques used in cache memory.	6	2	5
		OR			
11.	a).	Write a short note on flash memory.	6	3	5
	b).	Define locality of reference and explain use of a cache memory and direct –mapped cache.	6	3	5

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: BT24EC32P3A

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

BIO-MEDICAL INSTRUMENTATION

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	What are the basic objectives of a medical instrumentation system?	1	2	2
	b).	Define resting and action potentials.	1	2	2
	c).	Define ECG and mention its importance.	2	2	2
	d).	What are the components of the cardiovascular system?	2	2	2
	e).	What is intensive care monitoring?	3	2	2
	f).	List any two instruments used in respiratory system analysis.	4	2	2
	g).	What is bio-telemetry?	5	2	2
	h).	Name any two physiological parameters suitable for bio-telemetry.	5	2	2
	i).	What is the purpose of X-ray instrumentation in medical diagnostics?	6	2	2
	j).	Define electrical shock hazard.	6	2	2
					5 x 10 = 50 Marks
		UNIT-1			
2.	a).	List the major physiological systems of the human body.	1	2	5
	b).	What is the role of electrodes in biomedical instrumentation?	1	2	5
		OR			
3.	a).	Explain the significance of biomedical signals.	1	2	5
	b).	Mention any two types of bio-potential electrodes.	1	2	5
		UNIT-2			
4.	a).	Explain the working principle of a blood pressure measurement system.	2	3	5
	b).	What is the significance of PQRS and T waves in ECG?	2	3	5
		OR			
5.	a).	Define cardiac output and its measurement method.	2	2	5
	b).	What is plethysmography?	2	2	5
		UNIT-3			
6.	a).	What is the function of a pacemaker?	3	2	5

	b).	What are the elements of patient monitoring equipment?	**3**	**2**	**5**
		OR			
7.	**a).**	How is respiration analyzed in biomedical systems?	**4**	**3**	**5**
	b).	Explain the need for calibration in patient monitoring systems.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	List the main components of a bio-telemetry system.	**5**	**2**	**5**
	b).	What are implantable telemetry units?	**5**	**3**	**5**
		OR			
9.	**a).**	Mention any two tests carried out on blood in clinical laboratories.	**5**	**2**	**5**
	b).	What is the role of automation in clinical testing?	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	List the physiological effects of electrical current on the human body.	**6**	**2**	**5**
	b).	What is medical thermography used for?	**6**	**3**	**5**
		OR			
11.	**a).**	Name any two modern imaging techniques.	**6**	**2**	**5**
	b).	What methods are used for electrical accident prevention in hospitals?	**6**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: BT24EC32P3D

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

ARTIFICIAL INTELLIGENCE

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	What are AI techniques?	1	2	2
	b).	Define state space search with an example.	1	2	2
	c).	What is the difference between procedural and declarative knowledge?	2	2	2
	d).	Define predicate logic with an example.	2	2	2
	e).	Define non-monotonic reasoning.	3	2	2
	f).	State Bayes' theorem in the context of AI.	4	2	2
	g).	Define semantic nets with an example.	5	2	2
	h).	What is fuzzy logic? Mention one application.	5	2	2
	i).	What is the Mini-Max algorithm in game playing?	6	2	2
	j).	Define natural language processing (NLP).	6	2	2
					5 x 10 = 50 Marks
		UNIT-1			
2.	a).	Explain the characteristics of a production system.	1	2	5
	b).	What is generate-and-test method?	1	2	5
		OR			
3.	a).	Describe the concept of hill climbing search.	1	3	5
	b).	What is meant by means-ends analysis?	1	3	5
		UNIT-2			
4.	a).	What are Isa and instance relationships?	2	2	5
	b).	Distinguish between procedural and declarative knowledge.	2	3	5
		OR			
5.	a).	Explain simple fact representation in predicate logic.	2	3	5
	b).	What is logic programming in knowledge representation?	2	3	5
		UNIT-3			
6.	a).	Explain the concept of statistical reasoning.	3	2	5

	b).	What are Bayesian networks used for?	**3**	**3**	**5**
		OR			
7.	**a).**	Define Dempster-Shafer theory.	**4**	**3**	**5**
	b).	Differentiate between rule-based and probabilistic reasoning.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	What are frames in AI knowledge representation?	**5**	**2**	**5**
	b).	Explain the concept of conceptual dependency.	**5**	**3**	**5**
		OR			
9.	**a).**	What are scripts in slot-and-filler structures?	**5**	**2**	**5**
	b).	Compare weak and strong slot-filler structures.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	What is alpha-beta cut-off in game search?	**6**	**3**	**5**
	b).	List any two components of a planning system.	**6**	**2**	**5**
		OR			
11.	**a).**	What is the function of the Hopfield network?	**6**	**3**	**5**
	b).	Distinguish between symbolic AI and connectionist AI.	**6**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

VLSI DESIGN

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	What is the relation between I_{DS} and V_{DS} in MOSFET?	1	2	2
	b).	What is latch-up in CMOS circuits?	1	2	2
	c).	What is the purpose of using stick diagrams?	2	2	2
	d).	Draw the layout for the CMOS Inverter?	2	3	2
	e).	Define propagation delay in a CMOS inverter.	3	1	2
	f).	What is scaling and limitations of scaling?	4	1	2
	g).	List two static properties of Complementary CMOS.	5	1	2
	h).	What is the basic principle of Dynamic CMOS logic?	5	2	2
	i).	What is the significance of LUTs in FPGA?	6	2	2
	j).	Define Level Sensitive Scan Design (LSSD).	6	1	2
		5 x 10 = 50 Marks			
		UNIT-1			
2.	a).	Explain the CMOS fabrication steps with neat diagram?	1	3	6
	b).	Compare CMOS, Bi-CMOS and Bipolar Technologies?	1	3	4
		OR			
3.	a).	Illustrate the different forms of pull-up transistors in MOS inverter circuits. Also provide the voltage transfer characteristics for each of them?	1	3	6
	b).	What is latch-up in CMOS circuits? Explain its causes, effects, and prevention techniques?	1	2	4
		UNIT-2			
4.	a).	Draw the Stick Diagram of 2 input NOR gate using CMOS logic?	2	3	6
	b).	Explain about the Lambda based design rules for Transistor?	2	2	4
		OR			
5.	a).	Explain 2μm CMOS design rule for wires?	2	2	6
	b).	Explain about double poly CMOS rules?	2	3	4

		UNIT-3			
6.	**a).**	Explain the concept of sheet resistance (Rs) and how it is applied to MOS transistors and inverters?	**3**	**3**	**6**
	b).	Discuss limitations of scaling. Explain it on the substrate doping?	**3**	**3**	**4**
		OR			
7.	**a).**	What are inverter delays? Explain the factors that contribute to propagation delay in CMOS inverters?	**4**	**2**	**6**
	b).	Explain about limits due to sub threshold currents?	**4**	**3**	**4**
		UNIT-4			
8.	**a).**	Explain the working principle of Complementary CMOS logic. What are its key static properties?	**5**	**3**	**5**
	b).	Realize the implementation of two-input NOR gate using CMOS logic. Explain the associated operation by giving truth table?	**5**	**3**	**5**
		OR			
9.	**a).**	Design and Explain Multiplexer based Latches?	**5**	**2**	**6**
	b).	What is Pass Transistor Logic? Explain how logic gates can be designed using pass transistors?	**5**	**4**	**4**
		UNIT-5			
10.	**a).**	Explain Basic architecture of FPGA in detail?	**6**	**3**	**5**
	b).	Explain the key features of the Xilinx XC4000 FPGA family. How does it differ from other FPGA families?	**6**	**2**	**5**
		OR			
11.	**a).**	Explain logical stuck-at-0 or stuck-at-1 faults with the help of suitable examples?	**6**	**3**	**6**
	b).	Explain Built-In-Self Test (BIST) with the help of example?	**6**	**2**	**4**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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Course Code: BT24EC3203

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

DIGITAL SIGNAL PROCESSING

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	If X(z) is the z-transform of the signal x(n) then what is the ZT of anu(n) ?	1	2	2
	b).	Evaluate the Z-transform of $e^{3n}u(n)$?	1	2	2
	c).	What is the ROC of the z-transform of the signal x(n)=anu(n)+bnu(-n-1)	2	2	2
	d).	What is the DFT of the four-point sequence x(n)= {0,1,2,3}	2	2	2
	e).	What is the circular convolution of the sequences $X_1(n)=\{2,1,2,1\}$ and $x_2(n)=\{1,2,3,4\}$	3	1	2
	f).	What is the cut-off frequency of the Butterworth filter with a pass band gain p=-1 dB at p=4 rad/sec and stop band attenuation greater than or equal to 20dB at s=8 rad/sec?	4	2	2
	g).	List out the expressions for Hanning and Blackman window functions.	5	2	2
	h).	Illustrate the criteria for selecting window functions used in FIR filter design?	5	1	2
	i).	Which operation has to be performed to increase the sampling rate by an integer factor L?	6	1	2
	j).	Discuss about anti aliasing filter?	6	1	2

5 x 10 = 50 Marks

		UNIT-1			
2.	a).	Find the Z-transform of the signal x(n)=2n u(n)+3nu(-n-1) and its region of convergence.	1	3	5
	b).	Realize the series canonical realization of the following digital transfer function $X(Z) = \frac{z^2 + 2z + 4}{(z-8)(z^2 - 0.9z + 0.14)}$	1	2	5
		OR			
3.	a).	Compute the response of the following system to the input u(n). Discuss the stability of the given DT system?y(n)=0.7y(n-1)-0.12y(n-	1	2	5

		2)+x(n-1)+x(n-2)			
	b).	Find inverse Z-Transform of Find inverse Z-Transform of X(z)=(z^2+2z+3)/(z-1)(z-3)(z-4) for i) |z|>4 ii) |z|<1	1	4	5
		UNIT-2			
4.		Compute the DFT of the following sequence using Radix–2 DIT FFT algorithm. Show the all intermediate stage results: x(n)={0,1,2,0,2,1,0,2}	2	3	10
		OR			
5.		Obtain circular convolution of the two sequences given below using DFT approach x(n)={0,1,0,0}, h(n)={2,2,2,2}	2	3	10
		UNIT-3			
6.		Design digital Butterworth lowpass IIR filter using BLT method. The filter specifications are given by i) -3dB cutoff frequency at 0.5π rad, ii) at least 15dB attenuation at 0.75π rad	3	4	10
		OR			
7.	a).	Compare Chebyshev and Butterworth analog filters?	4	4	5
	b).	Convert the following analog filter with transfer function using impulse invariance method. HaS=s+0.2s+0.2)2+25	4	4	5
		UNIT-4			
8.		Design a linear-phase low pass FIR digital filter to meet the following specifications: (i) Pass band = 0 to 10 kHz (ii) Sampling frequency = 100 kHz, N=11. Compute the impulse response and transfer function of the desired FIR digital filter using Hamming window?	5	3	10
		OR			
9.	a).	Compare IIR and FIR digital filters?	5	3	5
	b).	Show that FIR filters provide constant group delay and phase delay?	5	4	5
		UNIT-5			
10.		Illustrate the operation of up-sampler, down-sampler, Interpolator and Decimator in time and frequency domains with neat sketches.	6	4	10
		OR			
11.	a).	Explain how Sub band coding of speech signals reduces the bit rate.	6	3	5
	b).	Discuss the effects of finite word length registers.	6	4	5

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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Course Code: BT24EC3202

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A) DR24

III B.Tech. II Semester MODEL QUESTION PAPER

MICROPROCESSORS AND MICROCONTROLLERS

Electronics and Communication Engineering

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	What are the three groups of signals in 8086?	1	1	2
	b).	What are the advantages of segmented memory?	1	1	2
	c).	Explain the difference between the ADD and ADDC instructions.	2	1	2
	d).	Give the register classification of 8086.	2	1	2
	e).	What is the significance of EA bar pin in 8051?	3	1	2
	f).	Explain PSW register?	4	2	2
	g).	Explain the role of the C/T bit in the TMOD register.	5	2	2
	h).	List the modes of timer in 8051.	5	2	2
	i).	Give different applications of ARM processors.	6	1	2
	j).	What is "Thumb" in ARM processor?	6	1	2
					5 x 10 = 50 Marks
		UNIT-1			
2.		Draw and explain the functional block diagram INTEL 8086 Microprocessor.	1	3	10
		OR			
3.	a).	Illustrate the generation of a 20-bit physical address in 8086 with an example.	1	3	5
	b).	Draw the flag register of 8086 and explain the function of each flag in detail.	1	2	5
		UNIT-2			
4.	a).	Draw the programmable register array of 8086 and explain the function of each Register.	2	2	5
	b).	Write an 8086-assembly language program to find the largest byte for a given block of bytes.	2	4	5
		OR			
5.	a).	Explain addressing modes of 8086 with suitable example.	2	3	5

	b).	Write an assembly language program for 8086 to find if given number is even or odd.	**2**	**3**	**5**

		UNIT-3			
6.		Outline the features and explain the internal block diagram of 8051 microcontroller.	**3**	**3**	**10**
		OR			
7.	**a).**	Explain memory organization in 8051 Microcontroller.	**4**	**2**	**5**
	b).	Classify the instructions of 8051 Microcontroller and Explain basic arithmetic Instructions.	**4**	**2**	**5**
		UNIT-4			
8.	**a).**	Explain TMOD and TCON register.	**5**	**2**	**5**
	b).	Explain Mode-1 programming of 8051 timer. Describe the different steps to program in Mode-1.	**5**	**3**	**5**
		OR			
9.	**a).**	With neat diagram write an assembly language program to interface ADC0808 to 8051 microcontrollers.	**5**	**3**	**5**
	b).	Write an assembly language program to generate a square wave on port pin P1.2 of 1kHz using timer-0 in mode 2.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain the various ARM families and their features.	**6**	**3**	**5**
	b).	Explain ARM core dataflow model with a neat diagram.	**6**	**3**	**5**
		OR			
11.	**a).**	With a neat diagram explain the different general purpose registers of ARM processors.	**6**	**2**	**5**
	b).	Explain current program status register (CPSR) with neat diagram.	**6**	**2**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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Course Code: BT24EC32P2B

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

SATELLITE COMMUNICATION

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	State any two applications of satellite communication systems.	1	2	2
	b).	What is meant by look angle determination in satellite communications?	1	2	2
	c).	What is the function of the Attitude and Orbit Control System (AOCS) in a satellite?	2	3	2
	d).	Define telemetry and state its purpose in satellite operation.	2	3	2
	e).	Define the C/N ratio and mention its importance in satellite link design.	3	4	2
	f).	What is system noise temperature? How does it affect link performance?	4	4	2
	g).	What is FDMA? Mention one disadvantage of FDMA	5	2	2
	h).	State the main function of an earth station antenna tracking system.	5	2	2
	i).	State any two differences between LEO and GEO satellite systems.	6	3	2
	j).	What is the basic principle of GPS location determination?	6	3	2
					5 x 10 = 50 Marks
		UNIT-1			
2.	a).	Discuss potential future developments in orbital mechanics and launch technologies that may revolutionize satellite deployment and maintenance.	1	2	6
	b).	Explain the concept of satellite constellations and their significance in enhancing global coverage and system redundancy.	1	2	4
		OR			
3.	a).	Discuss the methods and sensors used for determining the attitude (orientation) of a satellite in space. How is this information crucial for satellite operations?	1	2	6
	b).	Explain the role of battery systems in providing power during periods of eclipse or reduced solar exposure. How are these systems designed for reliability?	1	2	4
		UNIT-2			
4.	a).	Explain how external forces and perturbations affect a satellite's orbit and how the attitude and orbit control system compensates for these disturbances.	2	3	6
	b).	Discuss the components and technologies involved in the communication subsystem of a satellite. How is data transmitted between the satellite and Earth stations?	2	3	4
		OR			

5.	**a).**	Define system noise temperature in satellite communication systems. Explain its significance in determining the overall system noise performance.	**2**	**3**	**6**
	b).	Explain the basic principles of transmission theory in satellite communications. Discuss concepts such as modulation, bandwidth and signal to- noise ratio (SNR).	**2**	**3**	**4**
		UNIT-3			
6.		Describe the factors that affect signal propagation in satellite communication, including path loss, free-space loss and atmospheric effects. How do these factors impact signal quality?	**3**	**4**	**10**
		OR			
7.	**a).**	Discuss the concept of spread spectrum transmission and reception in CDMA systems. How does it enhance security and robustness in satellite communication?	**4**	**4**	**6**
	b).	Describe the components and features of receivers employed in Earth stations. How do they demodulate and process signals received from satellites?	**4**	**4**	**4**
		UNIT-4			
8.	**a).**	Explain the fundamental principles of Code Division Multiple Access (CDMA) in satellite communication. How does CDMA allow multiple users to share the same frequency band?	**5**	**2**	**5**
	b).	Explain the key components and characteristics of transmitters used in Earth stations. How is power amplification achieved, and what frequency bands are commonly used?	**5**	**2**	**5**
		OR			
9.		Explain the concept of Satellite Switched TDMA (SS-TDMA) and its advantages in dynamic allocation of satellite resources. Provide an example of SS-TDMA operation.	**5**	**2**	**10**
		UNIT-5			
10.		Explain the concept of Non-Geostationary Satellite Orbit (NGSO) constellations and their advantages over traditional GEO systems. What are the different NGSO constellation designs?	**6**	**3**	**10**
		OR			
11.		Discuss the operational challenges associated with NGSO constellation designs, including satellite handovers, tracking and ground station coordination.	**6**	**3**	**10**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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Course Code: BT24EC32P3C

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

EMBEDDED SYSTEMS

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	List two key characteristics of embedded systems.	1	1	2
	b).	Differentiate between Harvard and Von Neumann architectures.	1	2	2
	c).	What is the purpose of special registers in Cortex-M3?	2	2	2
	d).	Explain the significance of the memory map in Cortex-M3 architecture.	2	2	2
	e).	What is the difference between an interrupt and an exception?	3	1	2
	f).	How does NVIC help in reducing interrupt latency?	4	3	2
	g).	Define instruction syntax	5	1	2
	h).	What is the role of CMSIS in embedded system development?	5	2	2
	i).	What is an RTOS, and why is it used in embedded systems?	6	1	2
	j).	What are the different debug modes available in ARM Cortex-M3?	6	1	2

5 x 10 = 50 Marks

		UNIT-1			
2.	a).	Describe the RISC architecture and justify its use in ARM-based embedded systems.	1	3	5
	b).	Identify and explain the major challenges faced in embedded system design and development.	1	2	5
		OR			
3.	a).	Why is power efficiency crucial in embedded systems? Suggest techniques to reduce power consumption.	1	2	5
	b).	Describe various real-life applications of embedded systems across different domains.	1	2	5
		UNIT-2			
4.		Describe the architecture of Cortex-M3 with a labeled block diagram. Explain the role of each component	2	2	10
		OR			
5.	a).	Explain the different operation modes of Cortex-M3 and their significance in embedded applications.	2	1	5

	b).	Describe the pipeline mechanism in Cortex-M3. How does it improve instruction execution?	2	2	5
		UNIT-3			
6.		How does Direct Memory Access (DMA) reduce CPU workload? Discuss its advantages.	3	3	10
		OR			
7.	a).	What is the role of the Nested Vectored Interrupt Controller (NVIC)? Explain its features.	4	2	5
	b).	Describe the complete interrupt/exception sequence in Cortex-M3.	4	2	5
		UNIT-4			
8.	a).	Explain the concept of interrupt latency and the factors affecting it.	5	2	5
	b).	Evaluate the benefits of automatic stacking and unstacking during an exception in Cortex-M3.	5	3	5
		OR			
9.		Explain the CMSIS organization with a neat diagram.	5	2	10
		UNIT-5			
10.	a).	Explain the key debugging features of ARM Cortex-M3.	6	2	5
	b).	What is the Trace System in ARM Cortex-M3? Explain its components and working.	6	1	5
		OR			
11.	a).	Discuss how low-power design techniques optimize embedded system performance.	6	2	5
	b).	Explain the working and applications of the SYSTICK timer in ARM Cortex-M3.	6	2	5

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

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Course Code: BT24EC32P2D

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

MACHINE LEARNING

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	Compare Traditional Programming and Machine Learning approaches.	1	2	2
	b).	Distinguish between Quantitative and Qualitative data with examples.	1	2	2
	c).	Give an example for One-Hot-Encoding in feature engineering.	2	3	2
	d).	What is Principal Component Analysis (PCA) used for?	2	2	2
	e).	Give the formula for Linear Regression and explain its components.	3	3	2
	f).	List any four classification algorithms used in Supervised ML.	4	2	2
	g).	What are the differences between Hard and Soft Clustering?	5	2	2
	h).	Define Clustering. Give two real-world applications.	5	1	2
	i).	Mention two advantages of using Cross-Validation.	6	2	2
	j).	List any four evaluation metrics used for regression models.	6	1	2
		5 x 10 =50Marks			
		UNIT-1			
2.	a).	Explain the evolution and history of Machine Learning.	1	2	5
		Explain the concept of Machine Learning and how it differs from traditional programming with suitable examples.	1	2	5
		OR			
3.	a).	Describe quantitative and qualitative data types used in ML with real-world examples.	1	3	5
	b).	Explain Learning by Rote and Learning by Induction. Give an example for each to show the difference.	1	3	5
		UNIT-2			
4.	a).	Describe the steps involved in data cleaning and handling missing values and outliers.	2	3	5
	b).	Perform basic Exploratory Data Analysis (EDA) on a given dataset by identifying key patterns or insights and explain how it supports ML model building.	2	3	5
		OR			
5.	a).	Using a sample dataset, apply Univariate, Bivariate, and Multivariate	2	3	5

		analysis and interpret the visualizations or findings from each			
	b).	Given a dataset with categorical variables, perform Feature Engineering using One-Hot-Encoding and explain the resulting transformation.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Apply any one classification algorithm (e.g., Decision Tree or KNN) on a sample dataset and describe the outcome.	**3**	**3**	**5**
	b).	Given a dataset, identify whether it requires classification or regression and justify your choice with model implementation.	**3**	**3**	**5**
		OR			
7.	**a).**	Use a Random Forest Classifier on a dataset and explain how it improves accuracy compared to a single Decision Tree.	**4**	**3**	**5**
	b).	Train both Decision Tree and Logistic Regression models on a binary classification dataset and compare their confusion matrices.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	Given a dataset, apply both Hard Clustering (e.g., K-Means) and Soft Clustering (e.g., Gaussian Mixture Model) and compare the results	**5**	**3**	**5**
	b).	Apply K-Means clustering on a sample dataset and visualize the cluster assignments.	**5**	**4**	**5**
		OR			
9.	**a).**	Perform Agglomerative Hierarchical Clustering on a given dataset and represent the result using a dendrogram.	**5**	**3**	**5**
	b).	Apply any unsupervised learning technique (e.g., DBSCAN) on a real-world dataset and discuss practical challenges faced during implementation.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Given a confusion matrix for a binary classification problem, analyze how Accuracy, Precision, Recall, and F1-Score are calculated and interpret their significance in evaluating the model.	**6**	**4**	**5**
	b).	Analyze the difference between MSE and RMSE in regression by comparing their impact on model evaluation for datasets with outliers.	**6**	**4**	**5**
		OR			
11.	**a).**	Analyze the role of Stratified K-Fold Cross-Validation in handling imbalanced classification datasets and compare it with simple K-Fold validation.	**6**	**4**	**5**
	b).	Using a heatmap created from a multivariate dataset, analyze the correlations between features and discuss how this influences feature selection in ML models.	**6**	**4**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

Head
Department of ECE
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BHIMAVARAM-534 202

Course Code: BT24EC32P2C

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

SMART AND WIRELESS INSTRUMENTATION

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	**a).**	List any four classifications of sensors.	**1**	**1**	**2**
	b).	Write short notes on the evolution and history of WSN	**1**	**2**	**2**
	c).	Write a short note on the IMote node architecture.	**2**	**2**	**2**
	d).	Mention any two communication interfaces used in node architecture	**2**	**1**	**2**
	e).	What is source encoding	**3**	**1**	**2**
	f).	List different types of modulation used in WSN	**4**	**1**	**2**
	g).	What is Zigbee communication?	**5**	**1**	**2**
	h).	Write two energy management techniques.	**5**	**2**	**2**
	i).	How are seismic events sensed using WSN?	**6**	**2**	**2**
	j).	List any two WSN applications in healthcare.	**6**	**1**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the concept of Smart Instrumentation and its evolution with suitable examples	**1**	**3**	**5**
	b).	Describe the communication process in a WSN and its challenges	**1**	**3**	**5**
		OR			
3.	**a).**	Explain the various design constraints of a WSN — energy, self-management, and security.	**1**	**3**	**5**
	b).	Examine the aspects of decentralized management and wireless networking in a WSN	**1**	**3**	**5**
		UNIT-2			
4.	**a).**	Explain the architectural overview of a typical node in a WSN.	**2**	**3**	**5**
	b)	Compare microcontrollers, DSPs, ASICs, and FPGAs in node architectures.	**2**	**4**	**5**
		OR			
5	**a).**	Describe the working of the XYZ node architecture with a neat block	**2**	**3**	**5**

		diagram			
	b).	Discuss SPI and I2C communication interfaces used in WSN nodes.	**2**	**3**	**5**
		UNIT-3			
6.	**a).**	Explain the basic components of a wireless digital communication system.	**3**	**3**	**5**
	b).	Discuss information transmission over a channel and error recognition/correction.	**3**	**3**	**5**
		OR			
7.	**a).**	Describe Quadrature Amplitude Modulation with suitable diagrams.	**4**	**3**	**5**
	b).	Explain signal propagation and its challenges in wireless communication systems.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	Discuss the development of a WSN based on microcontroller and Zigbee.	**5**	**3**	**5**
	b).	Explain various energy harvesting methods and their principles.	**5**	**3**	**5**
		OR			
9.	**a).**	Describe different energy management techniques for battery-powered WSN nodes	**5**	**3**	**5**
	b).	Explain how battery selection is calculated for WSN applications.	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain single and multiple damage detection techniques using natural frequencies and mode shapes.	**6**	**3**	**5**
	b).	Describe precision agriculture and how WSN supports it	**6**	**3**	**5**
		OR			
11.	**a).**	Discuss the role of WSN in traffic control and healthcare monitoring.	**6**	**3**	**5**
	b).	Explain applications of WSN in underground mining and active volcano monitoring	**6**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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Course Code: BT24EC32P3B

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

MICROWAVE ENGINEERING

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	List the microwave applications.	1	2	2
	b).	Explain the probe and Loop.	1	3	2
	c).	List out the scattering properties.	2	2	2
	d).	Explain the significance of scattering matrix.	2	2	2
	e).	Classify microwave tubes.	3	1	2
	f).	Explain the slow wave structures.	4	2	2
	g).	Explain the negative resistance phenomenon.	5	2	2
	h).	What are the applications of solid sate devices?	5	1	2
	i).	List the blocks of microwave bench setup.	6	2	2
	j).	Define the VSWR?	6	1	2
					5 x 10 = 50 Marks
		UNIT-1			
2.	a).	Explain the operation of a Magic Tee and its applications in detail	1	3	5
	b).	State the principle of operation of Directional coupler. Explain the operation of two hole directional coupler in detail.	1	3	5
		OR			
3.	a).	Explain the operation of circulator	1	4	6
	b).	State Faraday rotation principle. Explain the operation of the isolator.	1	3	4
		UNIT-2			
4.	a).	What is a scattering matrix? Write the properties of a scattering matrix	2	3	5
	b).	Derive the S-parameters for Magic Tee.	2	3	5
		OR			
5.	a).	Show that the S' matrix of a perfectly matched 2-port network is $\begin{bmatrix} 00 \\ 10 \end{bmatrix}$	2	3	5
	b).	Explain the operations of directional coupler with the help s-parameters	2	3	5
		UNIT-3			

6.	**a).**	Explain the limitations of conventional tubes at Microwave frequencies in detail	**3**	**3**	**5**
	b).	Explain the working of Reflex klystron with neat diagram	**3**	**3**	**5**
		OR			
7.	**a).**	Explain the working of Helix travelling wave tube with neat diagram	**4**	**3**	**5**
	b).	Explain the working of 8-cavity Magnetron with neat diagram	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	Explain in detail the principle of operation of GUNN diode and detail different modes of operation of gunn diode.	**5**	**3**	**5**
	b).	Explain the operation IMPATT diode with suitable diagrams.	**5**	**3**	**5**
		OR			
9.	**a).**	Explain the operation TRAPATT diode with suitable diagrams	**5**	**3**	**5**
	b).	Explain the operation TUNNEL diode with suitable diagrams	**5**	**3**	**5**
		UNIT-5			
10.	**a).**	Explain the procedure with a neat diagram to measure the frequency and guide wave length	**6**	**3**	**5**
	b).	Explain the procedure for measurement of low and high VSWR with block diagram.	**6**	**3**	**5**
		OR			
11.		Draw the Block Diagram of Microwave bench setup and explain each block	**6**	**3**	**10**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 10 marks

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Course Code: BT24EC32P2A

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

ANALOG IC DESIGN

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	**a).**	What are the key parameters in a small-signal MOS transistor model?	**1**	**2**	**2**
	b).	Define sub-threshold conduction in a MOSFET.	**1**	**2**	**2**
	c).	What is the purpose of a beta helper in a current mirror circuit?	**2**	**2**	**2**
	d).	List two advantages of using a cascode current mirror.	**2**	**3**	**2**
	e).	What is the role of compensation in operational amplifier design?	**3**	**2**	**2**
	f).	Mention two differences between a differential amplifier and an inverter.	**4**	**3**	**2**
	g).	Define the term hysteresis in the context of comparators.	**5**	**2**	**2**
	h).	What is the key difference between a comparator and an operational amplifier?	**5**	**3**	**2**
	i).	What is a Voltage-Controlled Oscillator (VCO)?	**6**	**2**	**2**
	j).	Name two applications of Phase-Locked Loops.	**6**	**2**	**2**
					5 x 10 = 50 Marks
		UNIT-1			
2.	**a).**	Explain the significance of passive components in CMOS technology.	**1**	**2**	**5**
	b).	Describe the layout considerations in integrated circuits for MOS design	**1**	**2**	**5**
		OR			
3.	**a).**	Analyze the small-signal model of a MOS transistor for low-frequency applications.	**1**	**3**	**6**
	b).	Compare different computer simulation models used for MOS device analysis.	**1**	**2**	**4**
		UNIT-2			
4.	**a).**	Explain the function of a MOS switch and its practical limitations.	**2**	**2**	**5**
	b).	Describe how a current mirror with beta helper improves performance.	**2**	**2**	**5**
		OR			

5.	**a).**	Analyze the performance of a cascode current mirror in terms of output resistance and compliance voltage	**2**	**3**	**5**
	b).	Explain the principle of operation of a temperature-independent bandgap reference circuit	**2**	**2**	**5**
		UNIT-3			
6.	**a).**	Describe the operation of a differential amplifier and list its key performance parameters	**3**	**2**	**5**
	b).	Analyze the cascode operational amplifier configuration and explain how it improves power supply rejection ratio (PSRR).	**3**	**3**	**5**
		OR			
7.	**a).**	Explain the compensation techniques used in two-stage CMOS operational amplifiers.	**4**	**2**	**5**
	b).	Analyze the high gain amplifier architecture and its significance in analog ICs	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	Define the term comparator and list its important specifications	**5**	**2**	**5**
	b).	Analyze the design improvements to enhance speed and accuracy in open-loop comparators.	**5**	**3**	**5**
		OR			
9.	**a).**	Differentiate between two-stage and other open-loop comparators.	**5**	**3**	**5**
	b).	Explain how discrete-time comparators operate and where they are used.	**5**	**2**	**5**
		UNIT-5			
10.	**a).**	Explain the basic principle and frequency calculation of a ring oscillator.	**6**	**2**	**5**
	b).	Compare LC and ring oscillators in terms of phase noise and frequency stability.	**6**	**3**	**5**
		OR			
11.	**a).**	Describe the operation of a simple PLL and its building blocks.	**6**	**2**	**6**
	b).	Design a basic charge-pump PLL and analyze its non-ideal effects like jitter and lock time.	**6**	**4**	**4**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks

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Course Code: OE

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. II Semester MODEL QUESTION PAPER

OPERATING SYSTEMS

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	List any three major functions of an operating system.	1	1	2
	b).	What is meant by multiprogramming and time-sharing?	1	2	2
	c).	Define context switching. Why is it required?	2	1	2
	d).	What is the difference between a process and a thread?	2	2	2
	e).	What are semaphores? Differentiate between binary and counting semaphores.	3	2	2
	f).	Write the two processes of Peterson's solution for mutual exclusion	4	2	2
	g).	What is the Difference between contiguous and non-contiguous memory allocation.	5	2	2
	h).	Define thrashing and mention one method to avoid it.	5	2	2
	i).	Define file allocation table (FAT) and its purpose.	6	2	2
	j).	What is a protection ring, and how does it enhance system security?	6	2	2
				5 x 10 = 50 Marks	
		UNIT-1			
2.	a).	Identify the key components of an operating system with a neat diagram showing the interaction between user, OS, and hardware.	1	3	5
	b).	Name and explain the different types of system calls with suitable examples.	1	3	5
		OR			
3.	a).	Describe various operating system services that help users and programs interact with hardware.	1	3	5
	b).	Narrate the role of the user interface (CLI, GUI, touch-based) in OS design and give examples.	1	3	5
		UNIT-2			
4.	a).	Explain about Inter-Process Communication (IPC) using message passing and shared memory.	2	2	5
	b).	Illustrate parts of a Process Control Block (PCB) with neat sketch.	2	3	5
		OR			

<table>
<tr><td>5.</td><td>a).</td><td>Consider the following processes
<table><tr><th>Process</th><th>Arrival Time(ms)</th><th>Burst Time(ms)</th></tr><tr><td>P1</td><td>0</td><td>8</td></tr><tr><td>P2</td><td>1</td><td>4</td></tr><tr><td>P3</td><td>2</td><td>9</td></tr><tr><td>P4</td><td>3</td><td>5</td></tr></table>i) Construct the Gantt chart and calculate average waiting and turnaround time using FCFS (First Come First Serve) scheduling.
ii) Repeat the same using Round Robin (RR) scheduling with q = 3ms and compare which performs better.</td><td>2</td><td>3</td><td>10</td></tr>
<tr><td></td><td></td><td colspan="4">UNIT-3</td></tr>
<tr><td>6.</td><td>a).</td><td>Present the critical section problem. Explain the requirements of a solution to this problem and evaluate how different synchronization tools satisfy these requirements.</td><td>3</td><td>2</td><td>5</td></tr>
<tr><td></td><td>b).</td><td>Illustrate how resource allocation graphs can be used to represent and detect deadlocks.</td><td>3</td><td>3</td><td>5</td></tr>
<tr><td></td><td></td><td colspan="4">OR</td></tr>
<tr><td>7.</td><td>a).</td><td>Use the Banker's Algorithm to check if the system is in a safe state and find the safe sequence if exists
<table><tr><th>Process</th><th>Alloted</th><th>Max</th><th>Available = (3,3,2)</th></tr><tr><td>P1</td><td>(0,1,0)</td><td>(7,5,3)</td><td></td></tr><tr><td>P2</td><td>(2,0,0)</td><td>(3,2,2)</td><td></td></tr><tr><td>P3</td><td>(3,0,2)</td><td>(9,0,2)</td><td></td></tr><tr><td>P4</td><td>(2,1,1)</td><td>(2,2,2)</td><td></td></tr><tr><td>P5</td><td>(0,0,2)</td><td>(4,3,3)</td><td></td></tr></table></td><td>4</td><td>3</td><td>10</td></tr>
<tr><td></td><td></td><td colspan="4">UNIT-4</td></tr>
<tr><td>8.</td><td>a).</td><td>Discuss the working of paging and page table structure in a 32-bit address system.</td><td>5</td><td>2</td><td>5</td></tr>
<tr><td></td><td>b).</td><td>Compare First-Fit, Best-Fit, and Worst-Fit allocation strategies with advantages and disadvantages.</td><td>5</td><td>3</td><td>5</td></tr>
<tr><td></td><td></td><td colspan="4">OR</td></tr>
<tr><td>9.</td><td></td><td>Given a disk queue:
98, 183, 37, 122, 14, 124, 65, 67 and the current head position = 53.
i) Calculate the total head movement (in cylinders) for FCFS, SCAN (assuming movement toward higher cylinder numbers).</td><td>5</td><td>2</td><td>10</td></tr>
<tr><td></td><td></td><td colspan="4">UNIT-5</td></tr>
<tr><td>10.</td><td>a).</td><td>How a file system performs file creation, deletion and renaming operations. Elaborate.</td><td>6</td><td>4</td><td>5</td></tr>
<tr><td></td><td>b).</td><td>Write about the directory implementation techniques using linear list and hash tables.</td><td>6</td><td>2</td><td>5</td></tr>
<tr><td></td><td></td><td colspan="4">OR</td></tr>
<tr><td>11.</td><td>a).</td><td>Demonstrate the hierarchical directory structure and list its advantages in large systems.</td><td>6</td><td>3</td><td>5</td></tr>
<tr><td></td><td>b).</td><td>Explain the access matrix model for protection, illustrating how it enforces controlled access.</td><td>6</td><td>3</td><td>5</td></tr>
</table>

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks.

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DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR24

III B.Tech. I Semester MODEL QUESTION PAPER

ENTREPRENEURSHIP DEVELOPMENT & VENTURE CREATION

For ECE

Time: 3 Hrs. **Max. Marks: 70 M**

Answer Question No.1 compulsorily

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

10 x 2 = 20 Marks

			CO	KL	M
1.	a).	Define entrepreneurship and explain its essential features.	1	1	2
	b).	List two key differences between entrepreneurs and managers.	1	2	2
	c).	Identify what makes a customer problem "painful" enough to solve.	2	1	2
	d).	Explain why customer validation is important in the early stages of a startup.	2	2	2
	e).	Illustrate the role of a prototype in validating startup ideas.	3	2	2
	f).	Classify types of opportunities based on risk and return.	4	2	2
	g).	Compute the basic components of unit economics with examples.	5	2	2
	h).	Distinguish between direct and indirect Go-to-Market channels.	5	2	2
	i).	Critique why some startups fail to scale effectively.	6	2	2
	j).	Design a short 30-second elevator pitch for your idea.	6	2	2
				5 x 10 = 50 Marks	
		UNIT-1			
2.	a).	Describe how entrepreneurship contributes to national development.	1	3	5
	b).	Analyze the major sources of innovative startup ideas with examples.	1	3	5
		OR			
3.	a).	Describe Schumpeter's theory of innovation and its relevance today.	1	3	5
	b).	Analyze policy frameworks supporting Indian entrepreneurs.	1	3	5
		UNIT-2			
4.	a).	Compare customer discovery techniques and justify which is best for a new venture.	2	2	5
	b).	Illustrate the steps involved in identifying and validating a problem using design thinking.	2	3	5
		OR			
5.	a).	Apply design-thinking tools to identify customer problems.	2	3	5
	b)	Evaluate how customer interviews refine opportunity identification.	2	3	5

		UNIT-3			
6.	**a).**	Develop a prototype testing plan for a mobile app-based business.	**3**	**2**	**5**
	b).	Examine methods of opportunity sizing using TAM, SAM, and SOM.	**3**	**3**	**5**
		OR			
7.	**a).**	Design a prototype development cycle for a MedTech startup.	**4**	**3**	**5**
	b).	Examine opportunity evaluation through competitive benchmarking.	**4**	**3**	**5**
		UNIT-4			
8.	**a).**	Construct a business model canvas for an electric bike rental startup.	**5**	**2**	**5**
	b).	Assess how pricing and channel strategy influence the Go-to-Market plan.	**5**	**3**	**5**
		OR			
9.	**a).**	Discuss how revenue and cost models influence startup sustainability.	**5**	**2**	**5**
	b).	Construct a Go-to-Market strategy for an AI-based platform.	**5**	**2**	**5**
		UNIT-5			
10.	**a).**	Judge valuation metrics for early-stage vs. growth-stage ventures.	**6**	**4**	**5**
	b).	Develop a comprehensive investor pitch narrative.			
		OR			
11.	**a).**	Justify the scaling strategies suitable for hardware-based startups. [	**6**	**3**	**5**
	b).	Design a detailed investor pitch for your venture.	**6**	**3**	**5**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 10 marks.

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DR25
M.Tech
Model Papers

Course Code: D2513800

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

MATHEMATICAL FOUNDATION FOR COMMUNICATION ENGINEERING

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain sampling distributions and their importance.	1	2	6
	ii).	Discuss unbiasedness and minimum variance of point estimators with examples.	1	3	6
		OR			
1.B	i).	Explain the steps involved in one-sample hypothesis testing for mean.	1	3	6
	ii).	Compare one-sample and two-sample tests for mean with suitable illustrations.	1	4	6
		UNIT-2			
2.A	i).	Define Markov process and explain Markov chain with examples.	2	2	6
	ii).	Explain transition probability matrix and steady-state probabilities.	2	3	6
		OR			
2.B	i).	Define a random process and classify random processes.	2	3	6
	ii).	Explain random walk and determine its mean and variance.	2	3	6
		UNIT-3			
3.A	i).	Derive Bessel's interpolation formula and state its applicability.	3	3	6
	ii).	Explain Stirling's interpolation formula and compare it with Bessel's formula.	3	4	6
		OR			
3.B	i).	Explain the Newton–Raphson method for solving non-linear equations.	3	3	6
	ii).	Describe the fourth-order Runge–Kutta method for solving ODEs.	3	3	6
		UNIT-4			
4.A	i).	Explain necessary conditions for optimization of functions of several variables.	4	2	6
	ii).	Discuss sufficient conditions and nature of stationary points.	4	4	6
		OR			
4.B	i).	Explain constrained optimization using Lagrange multipliers.	4	3	6

	ii).	Solve an optimization problem using the Lagrange multiplier method.	4	4	6
		UNIT-5			
5.A	i).	Explain the concept of multi-resolution analysis.	5	2	6
	ii).	Describe continuous and discrete wavelet transforms.	5	3	6
		OR			
5.B	i).	Explain the role of wavelet transform in signal analysis.	5	4	6
	ii).	Discuss applications of wavelets in data compression and resolution enhancement.	5	5	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D2513801

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

DIGITAL SYSTEM DESIGN

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain Verilog as a Hardware Description Language. Discuss the levels of design description with suitable examples.	1	2	6
	ii).	Describe concurrency in Verilog and explain the difference between simulation and synthesis.	1	3	6
		OR			
1.B	i).	Write short notes on modules, system tasks, and parameters in Verilog HDL with examples.	1	4	6
	ii).	Explain the basic language constructs and conventions in Verilog HDL such as identifiers, numbers, logic values, and data types.	1	3	6
		UNIT-2			
2.A	i).	Explain the structure of a Verilog module and describe the AND gate primitive with syntax and example.	2	2	6
	ii).	Design a basic combinational circuit using gate-level modelling and explain its operation.	2	3	6
		OR			
2.B	i).	Explain tristate gates and array of instances of primitives with suitable examples.	2	3	6
	ii).	Design a D flip-flop using gate primitives and discuss delay and strength resolution.	2	3	6
		UNIT-3			
3.A	i).	Explain dataflow modelling in Verilog and describe continuous assignment statements with examples.	3	3	6
	ii).	Design a combinational logic circuit using operators and vector assignments at dataflow level.	3	4	6
		OR			
3.B	i).	Explain delays in continuous assignments and parameter usage in dataflow modelling.	3	3	6
	ii).	Write a Verilog program to implement a logic function using dataflow modelling and explain.	3	3	6
		UNIT-4			
4.A	i).	Explain the behavioral modelling approach and describe the 'initial' construct.	4	2	6

	ii).	Explain functional bifurcation and assignments with delays in behavioral modelling.	4	4	6
		OR			
4.B	i).	Explain the 'always' block and wait construct with suitable examples.	4	3	6
	ii).	Design a sequential circuit using multiple always blocks and explain its operation.	4	4	6
		UNIT-5			
5.A	i).	Differentiate between blocking and non-blocking assignments with examples.	5	2	6
	ii).	Explain the if–else and case statements used in Verilog procedural blocks.	5	3	6
		OR			
5.B	i).	Explain looping constructs in Verilog: for, while, repeat, and forever loops.	5	4	6
	ii).	Explain parallel blocks, force–release constructs, and events with suitable examples.	5	5	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D2513801

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

WIRELESS COMMUNICATIONS & NETWORKS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain the cellular concept and frequency reuse principle in cellular systems.	1	2	6
	ii).	Explain co-channel interference and adjacent channel interference. Discuss methods to improve system capacity.	1	3	6
		OR			
1.B	i).	Discuss channel assignment strategies and power control techniques used for reducing interference.	1	4	6
	ii).	Explain handoff strategies, prioritizing handoffs, and trunking with grade of service.	1	3	6
		UNIT-2			
2.A	i).	Explain the free space propagation model and two-ray ground reflection model.	2	2	6
	ii).	Describe the basic propagation mechanisms: reflection, diffraction, and scattering.	2	3	6
		OR			
2.B	i).	Explain Okumura and Hata propagation models with their applications.	2	3	6
	ii).	Discuss indoor propagation models and signal penetration into buildings.	2	3	6
		UNIT-3			
3.A	i).	Explain small-scale fading and the factors influencing small-scale fading.	3	3	6
	ii).	Explain Doppler spread, coherence time, and coherence bandwidth.	3	4	6
		OR			
3.B	i).	Describe the statistical models for multipath fading channels.	3	3	6
	ii).	Explain Rayleigh fading, level crossing rate, and average fade duration.	3	3	6
		UNIT-4			
4.A	i).	Explain the fundamentals of equalization in wireless communication systems.	4	2	6
	ii).	Describe LMS and RLS algorithms used for adaptive equalization.	4	4	6
		OR			

4.B	**i).**	Explain linear and non-linear equalizers with suitable block diagrams.	**4**	**3**	**6**
	ii).	Derive selection diversity improvement and maximal ratio combining (MRC).	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain WLAN architecture and IEEE 802.11 MAC protocol.	**5**	**2**	**6**
	ii).	Compare IEEE 802.11 a, b, g, and n standards.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain IEEE 802.16 and its enhancements.	**5**	**4**	**6**
	ii).	Discuss Wireless PANs, HiperLAN, and Wireless Local Loop (WLL).	**5**	**5**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D25138A0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

SOFTWARE DEFINED RADIO

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the need and characteristics of Software Defined Radio (SDR).	**1**	**2**	**6**
	ii).	Discuss the benefits and design principles of SDR.	**1**	**2**	**6**
		OR			
1.B	**i).**	Describe traditional hardware radio architecture used in early generation cellular systems.	**1**	**2**	**6**
	ii).	Explain SCR, SDR, ISR, and USR with neat block diagrams.	**1**	**2**	**6**
		UNIT-2			
2.A	**i).**	Explain the purpose of RF front-end in Software Defined Radio.	**2**	**2**	**6**
	ii).	Discuss dynamic range requirements and RF receiver front-end topologies.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain transmitter architectures used in software radio systems.	**2**	**3**	**6**
	ii).	Discuss noise and distortion sources in the RF chain and their impact on performance.	**2**	**3**	**6**
		UNIT-3			
3.A	**i).**	Compare Direct Digital Synthesis with analog signal synthesis.	**3**	**3**	**6**
	ii).	Explain different approaches to Direct Digital Synthesis with block diagrams.	**3**	**3**	**6**
		OR			
3.B	**i).**	Analyse the sources of spurious signals in Direct Digital Synthesis.	**3**	**4**	**6**
	ii).	Explain spurious components due to periodic jitter.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the principles of sample rate conversion.	**4**	**3**	**6**
	ii).	Discuss polyphase filters and their role in multirate signal processing.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain digital filter banks used in multirate systems.	**4**	**3**	**6**

	ii).	Describe timing recovery in digital receivers using multirate digital filters.	4	3	6
		UNIT-5			
5.A	i).	Explain ideal parameters of A/D and D/A converters.	5	2	6
	ii).	Discuss practical data converter parameters and techniques to improve performance.	5	3	6
		OR			
5.B	i).	Evaluate limitations of practical data converters in SDR systems.	5	4	6
	ii).	Explain the relevance of JTRS and its role in software radio systems.	5	3	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D25138A1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

OPTICAL COMMUNICATION & NETWORKS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	i).	Explain the elements of an optical fiber transmission link with a neat block diagram.	1	2	6
	ii).	Describe optical fiber structures, fiber types, and modes of propagation.	1	2	6
		OR			
1.B	i).	Explain step index and graded index fibers with ray diagrams.	1	2	6
	ii).	Discuss fabrication, cabling, and installation of optical fibers.	1	2	6
		UNIT-2			
2.A	i).	Explain the structure and working principle of LEDs used in optical communication.	2	2	6
	ii).	Discuss laser diode threshold condition and modulation capability.	2	3	6
		OR			
2.B	i).	Explain the working principles of PIN and APD photodiodes	2	3	6
	ii).	Compare optical detectors and discuss noise sources in photodetectors.	2	3	6
		UNIT-3			
3.A	i).	Draw and explain the block diagram of an optical communication system.	3	3	6
	ii).	Explain direct intensity modulation and digital optical communication systems	3	3	6
		OR			
3.B	i).	Describe the generations of optical fiber communication links.	3	4	6
	ii).	Explain 8 Mb/s and 2.5 Gb/s optical fiber communication links.	3	4	6
		UNIT-4			
4.A	i).	Explain fiber optic network components such as transceivers and optical amplifiers.	4	3	6
	ii).	Describe WDM systems and optical switches used in fiber optic networks.	4	3	6
		OR			
4.B	i).	Explain SONET/SDH architecture and wavelength routed optical networks.	4	3	6

	ii).	Discuss nonlinear effects and their impact on optical network performance.	4	3	6
		UNIT-5			
5.A	i).	Explain coherent optical receivers with homodyne detection.	5	2	6
	ii).	Discuss noise sources and polarization control in coherent receivers.	5	3	6
		OR			
5.B	i).	Explain heterodyne detection and laser line-width requirements.	5	4	6
	ii).	Describe synchronous, asynchronous, and self-synchronous demodulation techniques.	5	3	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D25138A2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

RADIO AND NAVIGATIONAL AIDS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain the radio positioning configurations and methods used in terrestrial navigation systems.	1	2	6
	ii).	Discuss the error sources and factors affecting positioning accuracy in radio positioning systems.	1	3	6
		OR			
1.B	i).	Explain the working principle of LORAN with its advantages and limitations.	1	2	6
	ii).	Describe the Instrument Landing System (ILS) and explain its role in aircraft navigation.	1	3	6
		UNIT-2			
2.A	i).	Define navigation and explain the concept of position fixing.	2	2	6
	ii).	Explain dead reckoning navigation and its applications in modern navigation systems.	2	3	6
		OR			
2.B	i).	Explain radio navigation and satellite navigation techniques.	2	2	6
	ii).	Describe the structure and working of a complete navigation system..	2	3	6
		UNIT-3			
3.A	i).	Explain the principle of Differential GNSS (DGNSS) and its accuracy improvement mechanism.	3	3	6
	ii).	Discuss carrier-phase positioning techniques used in satellite navigation.	3	4	6
		OR			
3.B	i).	Explain navigation challenges in poor signal-to-noise environments.	3	3	6
	ii).	Analyse multipath effects and describe multipath mitigation techniques.	3	4	6
		UNIT-4			
4.A	i).	Derive and explain inertial-frame and Earth-frame navigation equations.	4	3	6
	ii).	Explain local navigation frame equations used in inertial navigation systems.	4	4	6
		OR			

4.B	**i).**	Explain INS initialization and alignment methods.	**4**	**3**	**6**
	ii).	Analyse INS error propagation and its effect on navigation accuracy.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the fundamentals of GNSS systems such as GPS, GLONASS, Galileo, IRNSS.	**5**	**2**	**6**
	ii).	Discuss GNSS measurement errors including ionospheric, tropospheric, and multipath errors.	**5**	**4**	**6**
		OR			
5.B	**i).**	Explain Dilution of Precision (GDOP, PDOP) in satellite navigation.	**5**	**2**	**6**
	ii).	Analyse error correction techniques such as DGNSS, WAAS, and carrier-phase methods.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D25138B0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

FPGA and ASIC DESIGN

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	i).	Explain the evolution of programmable logic devices and the need for FPGAs.	1	2	6
	ii).	Describe the FPGA design flow and discuss major applications of FPGAs.	1	3	6
		OR			
1.B	i).	Explain the design of a universal logic block using PLDs.	1	3	6
	ii).	Describe the PLD-based design of a barrel shifter or memory block with suitable explanation.	1	3	6
		UNIT-2			
2.A	i).	Explain various FPGA/CPLD programming technologies.	2	2	6
	ii).	Compare SRAM, antifuse, and flash-based programming technologies.	2	3	6
		OR			
2.B	i).	Describe the architecture and features of Xilinx Spartan and Virtex FPGAs.	2	3	6
	ii).	Compare Altera and Actel FPGA/CPLD families with suitable examples.	2	3	6
		UNIT-3			
3.A	i).	Explain the Configurable Logic Block (CLB) functionality in FPGAs.	3	3	6
	ii).	Describe routing structures and I/O blocks used in FPGA architecture.	3	3	6
		OR			
3.B	i).	Analyse the impact of logic block functionality on FPGA performance.	3	4	6
	ii).	Explain the model used for measuring delay in FPGA architectures.	3	4	6
		UNIT-4			
4.A	i).	Explain routing terminology and general routing strategies in FPGAs.	4	3	6
	ii).	Describe routing in row-based FPGAs and segmented channel routing.	4	3	6
		OR			
4.B	i).	Explain the routing architecture of symmetrical FPGAs with an example.	4	4	6
	ii).	Discuss the general approach to routing in symmetrical FPGAs and independence from routing architectures.	4	4	6
		UNIT-5			

5.A	**i).**	Explain FPGA architectural assumptions and describe the logic block and connection block.	**5**	**3**	**6**
	ii).	Explain the switch block and switch block topology in FPGA architecture.	**5**	**3**	**6**
		OR			
5.B	**i).**	Analyse FPGA architectural features of Kintex-7, Virtex-7, and Artix-7 devices.	**5**	**4**	**6**
	ii).	Discuss real-world applications and case studies implemented using 7-series FPGAs.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D25138B1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

SYSTEM DESIGN WITH RTOS AND EMBEDDED LINUX

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the key characteristics of Real-Time Operating Systems (RTOS) and the role of the RTOS kernel and scheduler.	**1**	**2**	**6**
	ii).	Describe task management in RTOS, including task states, scheduling, and task operations.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain RTOS kernel objects, services, and system calls with suitable examples.	**1**	**2**	**6**
	ii).	Discuss task synchronization, communication, and concurrency issues in RTOS-based systems.	**1**	**3**	**6**
		UNIT-2			
2.A	**i).**	Explain semaphores and their operations. Discuss their use in inter-task synchronization.	**2**	**3**	**6**
	ii).	Describe message queues and other inter-process communication mechanisms such as pipes and signals.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain critical sections and resource synchronization methods in real-time systems.	**2**	**3**	**6**
	ii).	Analyse priority inversion, deadlocks, and common synchronization design problems in RTOS.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Define exceptions and interrupts. Explain their applications in real-time systems.	**3**	**2**	**6**
	ii).	Discuss spurious interrupts and their handling mechanisms in RTOS.	**3**	**4**	**6**
		OR			
3.B	**i).**	Explain timer services in RTOS, including real-time clocks and system clocks..	**3**	**2**	**6**
	ii).	Analyse the role of programmable interval timers and timer interrupt service routines in real-time applications.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the basics of Linux kernel and GNU utilities. Describe different Linux access methods.	**4**	**2**	**6**
	ii).	Describe commonly used Bash shell commands for navigation, file	**4**	**3**	**6**

		handling, and system monitoring.			
		OR			
4.B	**i).**	Explain the steps involved in shell script creation and basic control structures (if-else, loops).	**4**	**3**	**6**
	ii).	Discuss advanced shell scripting features such as signal handling, background scripts, and script functions.	**4**	**3**	**6**
		UNIT-5			
5.A	**i).**	Explain the embedded Linux architecture, including kernel, scheduler, memory manager, and file system.	**5**	**3**	**6**
	ii).	Describe the startup sequence and role of Board Support Package (BSP) in embedded Linux systems.	**5**	**3**	**6**
		OR			
5.B	**i).**	Analyse real-time Linux and hard real-time programming concepts in embedded systems.	**5**	**4**	**6**
	ii).	Explain the process of application porting and driver integration, including bootloader, kernel, root file system, and device tree.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D25138B2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. I Semester MODEL QUESTION PAPER

SYSTEM DESIGN USING VERILOG

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain Verilog as a Hardware Description Language and discuss the levels of design description.	1	2	6
	ii).	Explain concurrency in Verilog and describe the simulation and synthesis flow.	1	3	6
		OR			
1.B	i).	Describe Verilog language constructs and conventions such as data types, vectors and parameters.	1	2	6
	ii).	Explain operators, logic values and system tasks with suitable examples.	1	3	6
		UNIT-2			
2.A	i).	Explain gate-level modelling and describe basic gate primitives in Verilog.	2	2	6
	ii).	Explain tristate gates, delays and strengths used in gate-level modelling.	2	3	6
		OR			
2.B	i).	Design a flip-flop using gate primitives.	2	3	6
	ii).	Explain net types and construction resolution with examples.	2	4	6
		UNIT-3			
3.A	i).	Explain dataflow modelling and the concept of continuous assignment.	3	2	6
	ii).	Explain delays and vector assignments in continuous assignments.	3	3	6
		OR			
3.B	i).	Design a combinational circuit using dataflow modelling.	3	3	6
	ii).	Explain the use of parameters and constants in dataflow modelling.	3	4	6
		UNIT-4			
4.A	i).	Explain behavioural modelling and procedural assignments in Verilog.	4	2	6
	ii).	Explain the initial construct and always block with examples.	4	3	6
		OR			
4.B	i).	Explain assignments with delays and the wait construct.	4	3	6
	ii).	Explain the role of multiple always blocks in behavioural design.	4	4	6
		UNIT-5			

5.A	**i).**	Differentiate between blocking and non-blocking assignments.	**5**	**3**	**6**
	ii).	Explain if–else and case statements in Verilog.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain looping constructs: for, while, repeat and forever.	**5**	**3**	**6**
	ii).	Explain disable, parallel blocks, force–release and event control constructs.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D2523800

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

INFORMATION THEORY AND CODING

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Define information source and entropy. Derive the expression for entropy of a discrete random variable.	**1**	**2**	**6**
	ii).	Explain mutual information and joint & conditional entropy with suitable examples.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain information measures for continuous random variables.	**1**	**2**	**6**
	ii).	Discuss relative entropy and explain any two applications of information theoretic approach.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	State and explain the Source Coding Theorem and Kraft inequality.	**2**	**2**	**6**
	ii).	Explain the construction of Shannon–Fano and Huffman codes.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain Arithmetic coding and Run Length coding with examples.	**2**	**3**	**6**
	ii).	Describe the Lempel–Ziv–Welch (LZW) algorithm and explain the concept of universal source coding.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Define a communication channel and explain channel capacity.	**3**	**2**	**6**
	ii).	Derive the capacity of a discrete memoryless channel (DMC).	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain Gaussian channel and Binary Erasure Channel (BEC).	**3**	**2**	**6**
	ii).	Discuss MIMO channels and explain the effect of feedback on channel capacity.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the basics of video coding and describe quantization and symbol encoding.	**4**	**2**	**6**
	ii).	Explain intraframe coding and interframe coding techniques.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain transform coding and vector quantization used in image compression.	**4**	**3**	**6**

	ii).	Discuss speech coding principles including psycho-acoustic modelling and bit allocation.	4	4	6
		UNIT-5			
5.A	i).	Define Hamming weight and minimum distance. Explain error detection and correction theorems.	5	2	6
	ii).	Explain linear block codes, generator matrix and parity check matrix.	5	3	6
		OR			
5.B	i).	Explain cyclic codes and BCH codes with generator polynomials.	5	3	6
	ii).	Explain convolution codes and the Viterbi decoding algorithm.	5	4	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D2523801

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

IOT & ITS COMMUNICATION PROTOCOLS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the overall IoT architecture and describe the role of devices and gateways.	**1**	**2**	**6**
	ii).	Explain local and wide area networking in IoT and discuss data management in IoT systems.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain IoT technology fundamentals and the concept of M2M communication.	**1**	**2**	**6**
	ii).	Discuss Everything as a Service (XaaS) and the role of IoT analytics in business processes.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain the IoT reference architecture and describe the functional view.	**2**	**2**	**6**
	ii).	Explain the information view and deployment & operational view of IoT architecture.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain various architectural views used in IoT system design.	**2**	**2**	**6**
	ii).	Discuss real-world technical design constraints encountered in IoT implementations.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain IoT PHY/MAC layer technologies such as IEEE 802.11, IEEE 802.15 and 3GPP MTC.	**3**	**2**	**6**
	ii).	Explain Bluetooth Low Energy, Zigbee and Z-Wave protocols used in IoT.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain IPv6 and 6LoWPAN for IoT networking.	**3**	**2**	**6**
	ii).	Discuss IoT routing protocols such as RPL, CORPL and CARP.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain transport layer protocols TCP and UDP and their relevance to IoT.	**4**	**2**	**6**
	ii).	Explain the role of security protocols TLS and DTLS in IoT communication.	**4**	**3**	**6**
		OR			

4.B	**i).**	Explain session layer protocols HTTP and CoAP for IoT applications.	**4**	**3**	**6**
	ii).	Compare MQTT, AMQP and XMPP with respect to IoT communication requirements.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain IoT service layer protocols such as oneM2M and ETSI M2M.	**5**	**2**	**6**
	ii).	Explain the role of OMA and BBF standards in IoT interoperability.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain security challenges in IoT and the need for protocol-level security.	**5**	**2**	**6**
	ii).	Discuss security mechanisms in IoT protocols at MAC802.15.4, 6LoWPAN, RPL and application layer.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D2523802

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

EMBEDDED SYSTEM DESIGN

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	i).	Define an embedded system and compare embedded systems with general-purpose computing systems.	1	2	6
	ii).	Explain the characteristics and quality attributes of embedded systems with suitable examples.	1	3	6
		OR			
1.B	i).	Explain the history and classification of embedded systems.	1	2	6
	ii).	Discuss the major application areas and purpose of embedded systems.	1	4	6
		UNIT-2			
2.A	i).	Explain the core of an embedded system and describe general-purpose and domain-specific processors.	2	2	6
	ii).	Explain ASICs, PLDs and COTS components used in embedded systems.	2	3	6
		OR			
2.B	i).	Explain memory organization in embedded systems and discuss ROM and RAM types.	2	2	6
	ii).	Discuss sensors, actuators and communication interfaces (onboard and external) used in embedded systems.	2	4	6
		UNIT-3			
3.A	i).	Explain the need and operation of reset circuit and brown-out protection circuit in embedded systems.	3	2	6
	ii).	Explain the functions of oscillator unit, real-time clock and watchdog timer.	3	3	6
		OR			
3.B	i).	Explain the embedded firmware architecture and its key building blocks.	3	2	6
	ii).	Discuss embedded firmware design approaches and development languages.	3	4	6
		UNIT-4			
4.A	i).	Explain the ARM design philosophy and describe the ARM core architecture and registers.	4	2	6
	ii).	Explain the program status register (PSR) and instruction pipeline in ARM processors.	4	3	6

		OR			
4.B	**i).**	Explain ARM interrupts, vector table and operating modes.	**4**	**2**	**6**
	ii).	Explain ARM instruction sets: data processing, addressing modes, load/store and conditional instructions.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain the Raspberry Pi board architecture and its processor features.	**5**	**2**	**6**
	ii).	Explain programming the Raspberry Pi using Python.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain the communication interfaces of Raspberry Pi: I2C, SPI and UART.	**5**	**3**	**6**
	ii).	Discuss interfacing of sensors and actuators with Raspberry Pi for embedded applications.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D25238A0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

DESIGN FOR TESTABILITY

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the testing philosophy and the role of testing in VLSI systems.	**1**	**2**	**6**
	ii).	Explain fault modelling in digital circuits and describe the single stuck-at fault model.	**1**	**3**	**6**
		OR			
1.B	**i).**	Differentiate between functional testing and structural testing.	**1**	**2**	**6**
	ii).	Discuss VLSI technology trends affecting testing and types of testing.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain the need for simulation in design verification and test evaluation.	**2**	**2**	**6**
	ii).	Describe the true-value simulation algorithm with suitable examples.	**2**	**3**	**6**
		OR			
2.B	**i).**	Explain modelling of circuits for simulation in VLSI testing.	**2**	**2**	**6**
	ii).	Explain fault simulation algorithms used for test evaluation.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain SCOAP controllability and observability measures.	**3**	**2**	**6**
	ii).	Explain high-level testability measures used in digital circuits.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain ad-hoc DFT methods used to improve testability.	**3**	**2**	**6**
	ii).	Explain scan design and partial-scan design techniques.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain the economic motivation for BIST and describe the BIST process.	**4**	**2**	**6**
	ii).	Explain pattern generation and response compaction in logic BIST.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain random logic BIST and test-per-clock BIST systems.	**4**	**3**	**6**
	ii).	Explain memory BIST and delay fault BIST techniques.	**4**	**4**	**6**

		UNIT-5			
5.A	**i).**	Explain the motivation for boundary scan and describe the TAP controller and TAP port.	**5**	**2**	**6**
	ii).	Explain boundary scan test instructions and pin constraints of the standard.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain the boundary scan architecture used in board-level testing.	**5**	**2**	**6**
	ii).	Explain Boundary Scan Description Language (BSDL) and its description components.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D25238A1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

MEMS

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Differentiate between microsystems and MEMS. Explain the concept of integrated microsystems.	1	2	6
	ii).	Explain smart materials and discuss their applications in MEMS and microsystems.	1	3	6
		OR			
1.B	i).	Explain the basic concepts of microfabrication in MEMS.	1	2	6
	ii).	Discuss the structures and systems in MEMS and their application areas.	1	4	6
		UNIT-2			
2.A	i).	Explain the working principle of a silicon capacitive accelerometer.	2	2	6
	ii).	Explain the operation of a piezoresistive pressure sensor with neat diagrams.	2	3	6
		OR			
2.B	i).	Explain the working of an electrostatic comb-drive actuator.	2	2	6
	ii).	Discuss any two MEMS-based smart systems such as micro-mirror array, inkjet print head, or portable blood analyzer.	2	4	6
		UNIT-3			
3.A	i).	Explain silicon as a material for micromachining and its advantages.	3	2	6
	ii).	Explain thin-film deposition techniques used in MEMS fabrication.	3	3	6
		OR			
3.B	i).	Explain lithography and etching processes used in microfabrication.	3	2	6
	ii).	Discuss advanced microfabrication processes and specialized materials for microsystems.	3	4	6
		UNIT-4			
4.A	i).	Explain the mechanical modelling of a bar as a deformable element in MEMS.	4	2	6
	ii).	Explain the bending behaviour of beams using energy methods.	4	3	6
		OR			
4.B	i).	Explain heterogeneous layered beams and the bimorph effect	4	3	6

	ii).	Discuss residual stresses, Poisson effect, and anticlastic curvature in MEMS beams.	4	4	6
		UNIT-5			
5.A	i).	Explain the need for numerical methods and the basic concept of Finite Element Method (FEM).	5	2	6
	ii).	Explain the steps involved in FEM modelling of MEMS structures.	5	3	6
		OR			
5.B	i).	Explain the finite element model for structures with piezoelectric sensors and actuators.	5	2	6
	ii).	Discuss the FEM analysis of a piezoelectric bimorph cantilever beam.	5	4	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D25238A2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

SYSTEM ON CHIP DESIGN

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	**i).**	Explain the basic concepts of chips and System-on-Chip (SoC) ICs.	**1**	**2**	**6**
	ii).	Describe the major components of an SoC such as CPU/IP cores, coprocessors, cache and DRAM controller.	**1**	**3**	**6**
		OR			
1.B	**i).**	Explain the SoC design flow including synthesis, static timing analysis, verification and physical design.	**1**	**2**	**6**
	ii).	Discuss the role of design for testability (DFT) in SoC implementation.	**1**	**4**	**6**
		UNIT-2			
2.A	**i).**	Explain hardware–software partitioning in SoC design.	**2**	**2**	**6**
	ii).	Discuss area, time, power and cost trade-offs in hardware–software co-design.	**2**	**2**	**6**
		OR			
2.B	**i).**	Explain real-time scheduling issues in SoC-based systems.	**2**	**3**	**6**
	ii).	Explain the concept of hardware acceleration and its impact on system performance.	**2**	**4**	**6**
		UNIT-3			
3.A	**i).**	Explain virtual prototyping and its importance in system-level design.	**3**	**2**	**6**
	ii).	Explain transaction-level modeling (TLM) and electronic system-level (ESL) languages.	**3**	**3**	**6**
		OR			
3.B	**i).**	Explain the process of mapping high-level language applications to hardware.	**3**	**3**	**6**
	ii).	Discuss high-level synthesis (C-to-RTL) and source-level optimizations.	**3**	**4**	**6**
		UNIT-4			
4.A	**i).**	Explain bus-based interconnection structures in SoCs.	**4**	**2**	**6**
	ii).	Explain the features of AMBA AXI and AXI4-Stream protocols.	**4**	**3**	**6**
		OR			
4.B	**i).**	Explain Network-on-Chip (NoC) architecture and its advantages over buses.	**4**	**2**	**6**

	ii).	Discuss IP interfacing issues in NoC-based SoC systems.	4	4	6
		UNIT-5			
5.A	i).	Explain system-level modeling and integration in SoC design.	5	2	6
	ii).	Explain simulation platforms used for performance analysis of SoC/MPSoC.	5	3	6
		OR			
5.B	i).	Explain performance and power metrics used in SoC evaluation.	5	3	6
	ii).	Discuss use cases and examples for system-level performance and power analysis.	5	4	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D25238B0

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

DETECTION AND ESTIMATION THEORY

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

			CO	KL	M
		UNIT-1			
1.A	i).	Explain discrete linear models and their significance in modelling random processes.	1	2	6
	ii).	Discuss Markov sequences and Markov processes with suitable examples.	1	3	6
		OR			
1.B	i).	Describe point processes and their applications in signal processing.	1	2	6
	ii).	Explain the characteristics and properties of Gaussian random processes.	1	3	6
		UNIT-2			
2.A	i).	Explain the basic detection problem and derive the MAP decision rule.	2	3	6
	ii).	Describe the minimum probability of error classifier using Bayes decision theory.	2	3	6
		OR			
2.B	i).	Explain the Neyman–Pearson criterion for binary hypothesis testing.	2	3	6
	ii).	Discuss the general Gaussian detection problem and computation of probability of error.	2	4	6
		UNIT-3			
3.A	i).	Derive the linear minimum mean square error (LMMSE) estimator.	3	3	6
	ii).	Explain nonlinear MMSE estimation and the concept of innovations.	3	3	6
		OR			
3.B	i).	Explain the design and operation of digital Wiener filters with stored data.	3	3	6
	ii).	Describe the Kalman filter algorithm and its applications.	3	4	6
		UNIT-4			
4.A	i).	Explain nonparametric estimators of probability density functions.	4	2	6
	ii).	Discuss point estimators and measures of the quality of estimators.	4	3	6
		OR			
4.B	i).	Explain the concepts of interval estimation and distribution of estimators.	4	3	6
	ii).	Describe tests of hypotheses and explain simple linear regression.	4	4	6

		UNIT-5			
5.A	**i).**	Explain tests for stationarity and ergodicity of random processes.	**5**	**3**	**6**
	ii).	Discuss model-free estimation of random process parameters.	**5**	**3**	**6**
		OR			
5.B	**i).**	Explain model-based estimation of autocorrelation functions.	**5**	**3**	**6**
	ii).	Describe methods for estimating power spectral density functions from data.	**5**	**4**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D25238B1

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

EMI/ EMC

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain the electromagnetic environment and basic concepts of EMI and EMC.	1	2	6
	ii).	Discuss the history, practical experiences, and concerns related to EMI in engineering systems.	1	3	6
		OR			
1.B	i).	Describe the frequency spectrum conservation and its importance in EMC.	1	2	6
	ii).	Explain the natural and nuclear sources of EMI and their effects on electronic systems.	1	3	6
		UNIT-2			
2.A	i).	Explain electromagnetic emissions due to relays, switches, and non-linear circuit elements.	2	3	6
	ii).	Discuss passive intermodulation and crosstalk in transmission lines.	2	3	6
		OR			
2.B	i).	Explain transients in power supply lines and their role in EMI generation.	2	3	6
	ii).	Describe open area test sites (OATS) and methods used for EMI measurements.	2	4	6
		UNIT-3			
3.A	i).	Explain the construction and working of an anechoic chamber and TEM cell.	3	2	6
	ii).	Discuss characterization of conducted currents and voltages on power lines.	3	3	6
		OR			
3.B	i).	Explain conducted EMI from equipment and methods of immunity measurement.	3	3	6
	ii).	Describe Electrostatic Discharge (ESD), EFT/bursts, and electrical surge phenomena.	3	3	6
		UNIT-4			
4.A	i).	Explain the principles and types of grounding used in EMC applications.	4	2	6
	ii).	Discuss shielding and bonding techniques for EMI control.	4	3	6

		OR			
4.B	**i).**	Explain the characterization of EMI filters.	**4**	**3**	**6**
	ii).	Describe the design of power line filters for EMI suppression.	**4**	**4**	**6**
		UNIT-5			
5.A	**i).**	Explain EMI suppression cables and EMC connectors.	**5**	**2**	**6**
	ii).	Discuss the role of EMC gaskets, isolation transformers, and opto-isolators.	**5**	**3**	**6**
		OR			
5.B	**i).**	Describe the need and importance of EMC standards.	**5**	**2**	**6**
	ii).	Explain national and international EMC standards with examples.	**5**	**3**	**6**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202.

Course Code: D25238B2

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

I M. Tech. II Semester MODEL QUESTION PAPER

ARM CONTROLLERS AND EMBEDDED C

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Explain the ARM design philosophy, register organization, and CPSR with suitable diagrams.	1	2	6
	ii).	Discuss the ARM instruction set covering data processing, load–store, branch, and PSR instructions.	1	3	6
		OR			
1.B	i).	Describe the Thumb instruction set, register usage, and advantages over ARM instructions.	1	2	6
	ii).	Explain efficient C programming techniques and ARM assembly code optimization methods.	1	4	6
		UNIT-2			
2.A	i).	Explain exception and interrupt handling mechanisms in ARM processors with vector table.	2	3	6
	ii).	Discuss the ARM memory hierarchy and cache architecture, including cache policies.	2	3	6
		OR			
2.B	i).	Explain the Memory Protection Unit (MPU) and its initialization in ARM systems.	2	3	6
	ii).	Describe the ARM Memory Management Unit (MMU), virtual memory concept, and TLB.	2	4	6
		UNIT-3			
3.A	i).	Explain the ARM Cortex-M architecture and instruction categories with examples.	3	2	6
	ii).	Discuss branching, conditional execution, and subroutines in ARM Cortex-M.	3	3	6
		OR			
3.B	i).	Explain GPIO input/output modes and memory-mapped I/O with push-button interfacing.	3	4	6
	ii).	Describe the working and configuration of general-purpose timers and PWM generation.	3	4	6
		UNIT-4			
4.A	i).	Explain the UART block, registers, and baud rate calculation in ARM Cortex-M.	4	3	6

	ii).	Describe UART initialization and data transmission/reception with suitable flow.	4	4	6
		OR			
4.B	i).	Explain ADC architecture, modes of operation, and configuration in ARM microcontrollers.	4	3	6
	ii).	Discuss interfacing of LCD / keypad / seven-segment display with ARM Cortex-M.	4	4	6
		UNIT-5			
5.A	i).	Explain the I²C protocol, operating modes, and configuration steps in ARM controllers.	5	3	6
	ii).	Describe sensor interfacing using I²C with a suitable example.	5	4	6
		OR			
5.B	i).	Explain the SPI protocol, modes of operation, and master–slave communication.	5	3	6
	ii).	Discuss the Smart Home – Smart Door Lock case study using ARM Cortex-M.	5	4	6

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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Head
Department of ECE
D.N.R. College of Engg. & Tech
BHIMAVARAM-534 202

Course Code: D2530000

DNR COLLEGE OF ENGINEERING & TECHNOLOGY(A)

DR25

II M. Tech. III Semester MODEL QUESTION PAPER

RESEARCH METHODOLOGY AND IPR

For Digital Electronics & Communication Systems

Time: 3 Hrs. **Max. Marks: 60 M**

Answer **ONE Question** from **EACH UNIT**

Assume suitable data if necessary

5 x 12 = 60 Marks

		UNIT-1	CO	KL	M
1.A	i).	Discuss use cases and examples for system-level performance and power analysis.	1	2	6
	ii).	Elaborate on common errors committed by researchers in selecting the research problem.	1	3	6
		OR			
1.B	i).	Give a detailed account on various approaches adopted by researchers in solving problems stated by them.	1	2	6
	ii).	Explain with neat sketches, various charts used in presentation of data.	1	4	6
		UNIT-2			
2.A	i).	What are the different ethical issues related to authorship?	2	2	6
	ii).	List and explain the guidelines for Effective technical writing.	2	3	6
		OR			
2.B	i).	List and elaborate the different sources of literature studies.	2	2	6
	ii).	How will you prepare the timeframe, activity schedule, budget plan for your proposed research?	2	4	6
		UNIT-3			
3.A	i).	List the different considerations in choosing a particular research contribution for patenting.	3	2	6
	ii).	What is IPR? Give examples.	3	3	6
		OR			
3.B	i).	Elaborate the concepts of creativity and innovation.	3	2	6
	ii).	Explain how patents are filed under PCT.	3	4	6
		UNIT-4			
4.A	i).	What is the transfer of technology in patent rights? Explain	4	2	6
	ii).	How patent information's are protected? Discuss.	4	3	6
		OR			
4.B	i).	Explain Geographical Indications.	4	3	6

	ii).	What is the information that can be gathered from patent database? Discuss.	4	4	6
		UNIT-5			
5.A	i).	Explain the Emerging issues in IPR.	5	2	6
	ii).	Describe the administration of Patent system.	5	3	6
		OR			
5.B		Discuss in detail about IPR of Biological Systems.	5	2	12

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 12 marks

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